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METAL-OXIDE THIN FILM TRANSISTORS BY SOL-GEL METHOD

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"I hereby declare that this thesis has been conducted in accordance with international ethical and academic standards of conduct and intellectual property protection. According to these standards, I have not engaged in plagiarism and have fully cited all sources used in this work."

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Abstract

The electronics industry has seen a significant surge in demand for semiconductor materials, driving researchers to explore active semiconductors that can address the growing needs of this sector. The primary objective of this research is to develop large-scale, green, and sustainable technologies for electronic applications, emphasizing low-cost solutions with minimal environmental impact. Metal oxides have emerged as promising candidates for electrical and optoelectronic applications due to their excellent electrical properties, including high charge density, optical transparency, ease of processing, stability, and affordability. Among these materials, indium oxide (In_2O_3) stands out as a potential candidate for developing thin-film transistors because of its high carrier mobility, low processing temperatures, strong electrical uniformity, visible light transparency, and cost-effectiveness. Initially, metal oxide thin-film transistors were fabricated using vacuum processes. However, the increasing demand for low-cost, high-throughput production with better compositional control has shifted focus toward solution-based processing methods. Solution processing, characterised by its simplicity, affordability, and scalability for large-area electronics, has gained significant attention. Over the past decade, solution-processed metal oxides have proven to be excellent candidates for thin-film transistors, offering functional components like conductors, semiconductors, and high-k dielectrics, especially for flexible and large-area electronics. Sol-gel technology has been widely investigated for producing MOs, ceramics, and glasses due to its ability to operate at significantly lower temperatures compared to traditional methods. The sol-gel process involves forming a solid-phase network through polymerization and polycondensation of precursors. Solution-processed thin-film transistors hold great promise for flexible, low-cost, and large-area electronics, presenting unique advantages over conventional silicon-based MOSFETs. Devices fabricated directly via solution processing or precision printing represent a new paradigm in manufacturing methods. In this study, the devices were fabricated in a bottom-gate, top-contact configuration, using doped p-type silicon wafer substrates with a 200 nm thick silicon dioxide layer as the gate dielectric. The In_2O_3 films were synthesised via the sol-gel method using indium nitrate hydrate ($In(NO_3)_3 \cdot xH_2O$) dissolved in 2-methoxyethanol (2-ME). The precursor solution was dispensed on top of the SiO_2 gate dielectric and spin-coated to form a uniform layer. A post-deposition thermal annealing step (300°C /1h) was employed to convert the precursor film into a metal oxide layer. Metal contacts were fabricated in the final step using e-beam evaporation. Optical reflectance measurements were conducted to determine the film thickness, and the study focused on the electrical characterisation of the resulting TFTs. The findings underscore the potential of solution-processed In_2O_3 films for next-generation flexible and sustainable electronics.

1. Introduction

In the past decade, incorporating new materials and methods into electronics manufacturing has sparked a technological shift, opening the door to innovative applications like flexible displays,[1] highly sensitive sensors,[2,3] memory devices,[4] and energy generation systems.[5] Seen as key technologies for the future, these applications largely rely on metal oxides (MOs) because of their unique properties—optical transparency, high carrier mobility, and mechanical durability/stability – that make them advantageous over traditional silicon- and organic-based technologies. Thin-film devices built with MOs, including Thin Film Transistors (TFTs), have become a growing area of scientific interest. Their compatibility with complementary metal-oxide-semiconductor (CMOS) technology is crucial for realizing the Internet of Things (IoT).[6] Metal oxide TFTs have been widely investigated as essential components for upcoming display technologies, thanks to their high electron mobility, strong on/off current ratios, and superior optical qualities. Traditionally, metal oxide TFTs were produced using vacuum-based methods like magnetron sputtering, atomic layer deposition, and pulsed laser deposition. However, with growing requirements for cost-effectiveness, precise compositional control, and efficient large-scale production, solution processing methods have gained significant attention. Using solution-based deposition of sol-gel metal oxide materials offers a cost-effective alternative, enabling large-area printing techniques that can effectively lower both material and processing costs.[7]

1.1 Motivation and Challenges

Metal-oxide-based electronics open up a wide range of valuable and cutting-edge applications by combining the “three foundational traits” of ideal materials: transparency, adjustable optoelectronic properties, and stability.[8] However, expanding this technology further depends heavily on reducing production costs and enhancing scalability. A significant barrier to achieving these goals lies in the continued use of traditional deposition methods, such as vacuum-based processes. While these methods produce high-quality metal-oxide thin films, their high costs and energy demands limit their feasibility for large-scale, affordable electronics. In contrast, solution-processed metal-oxide thin films present several benefits, including operation under atmospheric pressure, lower raw material expenses, and reduced operating costs. Additionally, solution-based techniques tend to be more environmentally friendly, generating less waste than conventional methods. The growing shift in materials fabrication research toward solution-based processes strengthens the potential of metal oxides to fulfil their promise as cost-effective, high-performance options for electronic devices. The incorporation of metal oxides into solution processes is accomplished through a technique known as “sol-gel.” This method offers a straightforward way to create MO thin films. It begins with metal-organic precursor salts, which, through inorganic polymerization reactions, form an oxide network.[9] These reactions take place by dissolving the precursor salts in solvents to create solutions, which are then applied to the desired substrates. Thus, “sol-gel processing” refers to synthesizing metal oxides using “wet chemistry” methods. The sol-gel technique is cost-effective and offers important benefits, such as customizable composition and the ability to operate under ambient conditions,

making it an accessible approach for developing “tailored” materials.[10] However, successfully utilizing the sol-gel process requires precise control over every chemical step involved. Among the diverse range of available metal-oxide (MO) semiconductors, indium oxide (In_2O_3) has recently gained attention due to its high electron mobility,[11] excellent optical transparency, and functionality as a transparent conducting oxide host. In addition to semiconductors, metal-oxide dielectrics like Al_2O_3 have emerged as top materials for optoelectronic applications, such as dielectric layers in TFTs, due to their high dielectric constant, broad bandgap, and high refractive index. Through sol-gel methods, metal oxides hold promise for enabling high-throughput manufacturing of high-performance devices using ultra-thin MO films. Achieving this goal relies on precise control of thin-film production through sol-gel processing. A variety of precursor salts, such as nitrates, acetates, and perchlorates, have been used to create metal-oxide thin films, each following specific chemical reaction paths toward MO formation, with precise temperature and atmospheric conditions required for effective treatment.[12] The rising demand for large-area, flexible, and low-cost electronics for unconventional displays, wearable technology, ultralight devices, and disposable circuits is driving the need for advanced electronic materials and cost-effective production methods. Metal oxide materials have emerged as a strong candidate in this field, demonstrating significant potential for use in transparent electrodes, high-mobility semiconductors, and high-k dielectrics. Using sol-gel chemistry, these metal oxides can be conveniently synthesized from small molecular precursors through straightforward solution-based processes, paving the way for very large-area electronics that are affordable and efficient to produce.[13] This aligns well with initiatives like the European Chips Act, which represents a strategic effort to bolster the semiconductor industry within the European Union, address the growing demand for advanced electronics, and enhance the region's technological sovereignty. The Act seeks to reduce reliance on non-EU suppliers and ensure a robust supply chain for microelectronics. By enhancing the capacity for local semiconductor production, the European Chips Act aims to facilitate the delivery of essential applications, from the Internet of Things (IoT) to renewable energy technologies, ensuring Europe remains competitive in the rapidly evolving global digital landscape.[14]

1.2 Research Aim

The aim of this study is to fabricate thin-film transistors (TFTs) with sol gel technique and analyse their electrical behaviour through the calculation of parameters such as threshold voltage, on/off ratio, and mobility. Additionally, the goal is to perform a statistical analysis to determine if transistors produced under identical methods and conditions exhibit any variations.

1.3 Research Objectives

1. The primary objective of this study is to fabricate thin-film transistors using the sol-gel technique for the deposition of thin films and e-beam evaporation for the fabrication of metal contacts.

2. Electrical characterisation by means of acquiring the transfer and output characteristics of the TFTs. This comprehensive characterisation is intended to deepen the understanding

of the electrical performance of sol-gel-based thin-film transistors and the impact of fabrication techniques on their functionality. Key parameters such as threshold voltage, sub-threshold voltage swing, on/off current ratio, and charge carrier mobility are calculated to evaluate the performance and reliability of the devices.

3. A further objective is to identify any systematic or random variations among transistors and understand their implications for large-scale production and application. The study aims to assess the uniformity and consistency of the devices produced under identical conditions, providing valuable insights into their reproducibility and potential sources of variation.

1.4 Overview of Research Methodology

The process involves preparing a solution through the dilution of precursor salts in a chosen solvent. This step ensures that the metal precursors are evenly distributed, creating a uniform mixture essential for the deposition phase. The viscosity of the solution, influenced by the molar concentration, is a key parameter that will later affect film thickness during deposition. The prepared solution is applied to the substrate through spin coating. During this process, the solution is dispensed on the substrate, which is rapidly spun to spread the material and form a uniform thin film. This step relies on controlling parameters like spinning speed, solution viscosity, and surface tension. Following spin coating, thermal annealing is used to eliminate any remaining solvent and promote inorganic polymerization, which transforms the precursor film into a metal oxide layer. Finally, Aluminum electrodes are deposited employing e-beam evaporation and patterned through a shadow mask to create the electronic contacts (source-drain) on top of the insulators. The back of the substrate is used as the gate electrode, thus the wafer is appropriately scratched to remove the native oxide and subsequently an Aluminum electrode is deposited via e-beam evaporation at the entire back surface of the Si wafer. The electrical properties of the fabricated thin-film transistors are evaluated by measuring the transfer and output characteristics of the TFTs. This three-pilar methodology ensures precise formation, transformation, and assessment of the metal oxide thin films, critical for creating efficient thin-film transistors using solution processing and sol-gel techniques.

2. Background and Literature Review

2.1. Device structure and operation

Thin Film Transistors (TFTs) are three-terminal field-effect devices that work by modulating current flowing through a semiconductor between two electrodes (source and drain). In this work, the architecture that is used is the Bottom Gate Top Contact architecture. Figure 1(a) shows the top view and Figure 1(b) shows the cross-section view of the TFT. A dielectric layer is inserted between the semiconductor and a transversal electrode (gate) (G), resulting in current modulation via capacitive injection of carriers near the dielectric/semiconductor interface, known as the field effect.[1] In other words, the source (S) and drain (D) electrodes inject or extract charge carriers, while the gate electrode controls the source-to-drain charge conduction. The source and drain electrodes typically contain a conductive material. The

semiconductor-based active layer is in contact with these materials. Additionally, conductive material in contact with the gate-insulating layer forms the gate electrode. The gate bias can modulate the charge flow through the semiconducting channel between the source and drain electrodes, resulting in polarization in the dielectric layer.[2] Stability is essential for both designing and using a device because its electrical properties can change over time due to environmental factors and aging.[3]

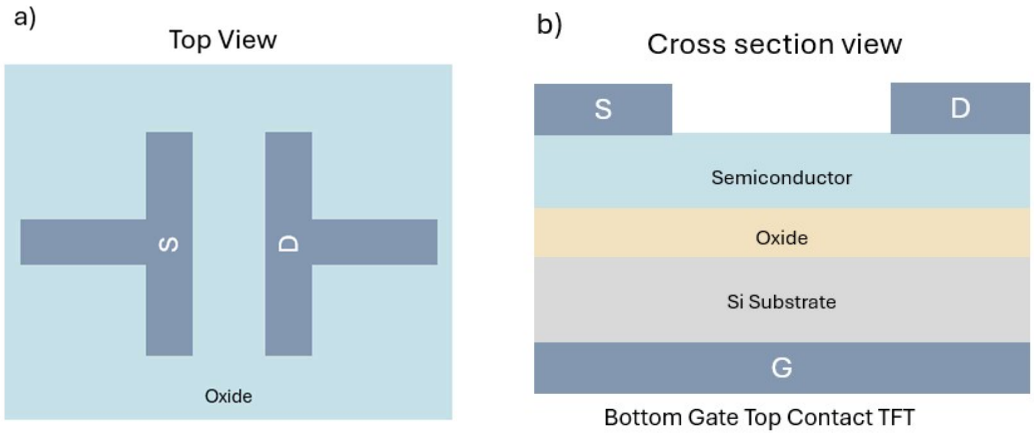


Figure 1. *a) Top view and b) Cross section view of a Bottom Gate Top Contact TFT*

2.1.1. Structure

Numerous combinations of semiconductor and insulating materials, electrode conductive materials, and substrates from operational TFT devices are presented. In terms of device structure, TFTs commonly use glass, plastic, or stainless-steel plates as substrates, with semiconductor thin films serving as active surface layers. TFTs are produced on top of the insulating layer using typical techniques including sputtering, sublimation, or inkjet printing. Depending on the application, the materials and procedures used may vary. The design architecture for a TFT includes four key sections: a gate electrode, a gate-insulating layer, an active layer, and source-drain electrodes. Typically, the source and drain electrodes are made of metals. These are in contact with the active layer, which is made of a semiconducting material. The gate electrode is also made of metal. Since the device's electrical properties might change over time due to aging and environmental factors, stability is essential when designing and using TFTs. Hysteresis, a phenomenon in which the device's current-voltage relationship varies when the voltage increases or lowers, is another important aspect influencing device performance. As a result, TFT's stability and hysteresis must be investigated to assure long-term performance and reliability.[3] TFTs can be built in a variety of configurations, which are presented in Figure 1 and Figure 2. The typical structures are bottom-gate top-contact (BGTC) (Figure 1(b)) , top-gate bottom-contact (TGBC) (Figure 2(a)), top-gate top-contact (TGTC) (Figure 2(b)), bottom-gate bottom-contact (BGBC) (Figure

2(c)). The usages and advantages of each configuration differ. In this work, bottom-gate top-contact TFTs are fabricated. A detailed explanation of the methodology follows in Chapter 3. BGTC is a popular configuration employed for MOS-based TFTs, due to the following reasons: The top source/drain electrodes are easily connectable, and the bottom gate electrode can be connected to other components. Many TFTs were proposed based on this structure.[5]

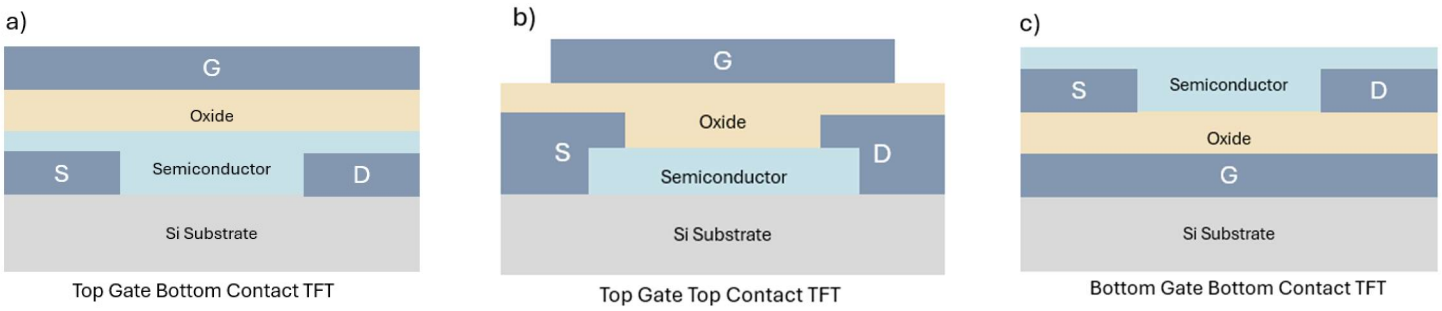


Figure 2. *Typical structure of TFT architectures. a) TGBC b) TGTC c) BGBC*

TFTs are very similar to other field-effect devices in terms of operation and composing layers, such as the well-known MOSFETs used in high-performance applications. However, significant differences exist between these devices as it is shown in Figure 3 , some of which are readily apparent when inspecting their typical structures.[1] A MOSFET operation is defined by the npn (or pnp) source-semiconductor-drain area, where the channel is formed during the inversion mode. Although, the channel conduction path in the TFT is simpler, following a metal (source)-semiconductor-metal (drain) structure. As a result, TFTs are activated in the accumulation region of operation. A MOSFET structure consists of a gate-oxide-semiconductor stack, as well as two highly doped areas (source and drain) within the semiconductor body. In contrast, a TFT structure can vary depending on the device's desired use. The main components of a TFT, namely the gate, dielectric, semiconductor, and source and drain, can be combined in a variety of stack configurations that are frequently determined by the application. In TFTs, the source and drain layers are represented by conductor materials (typically metals), rather than highly doped semiconductor areas like in MOSFETs.[7] A detailed discussion about the operation of TFTs is presented in the next paragraph.

2.1.2. Operation

The TFT operational characteristics are the current measurements when the TFT electrode is loaded with voltage. This process establishes the connection between the current and voltage implemented across the TFT (Figure 3(a)). Unlike MOSFETs (Figure 3(b)), which rely on inversion for conduction, thin-film transistors typically operate in the accumulation regime. In this mode, charge carriers accumulate at the semiconductor-insulator interface, modulating conductivity without requiring a bulk inversion layer. Hence, the standard TFT operational characteristic curves typically include transfer and output characteristic curves. The transfer curve is the most used operating parameter for TFT devices. The transfer curve

is determined using electrical measurements of the drain current-gate voltage (I_{DS}-V_{GS}) relationship, while the drain voltage (V_{DS}) remains constant throughout. Furthermore, the TFT's characteristic output curve is measured using the drain current-drain voltage (I_{DS}-V_{DS}) relationship obtained through electrical measurement while keeping V_{GS} constant. The following TFT static characteristics are extracted from the output (a) and transfer (b) characteristics shown in Figure 4 [1] : mobility (μ), on/off ratio, turn-on voltage (V_{ON}), threshold voltage (V_T), and subthreshold swing (SS). Each parameter is important in defining TFT devices, so it is explained separately in the following section.[3] Further details regarding the computational methods employed in this study, as well as the techniques used for constructing the relevant characteristics, are discussed in a subsequent chapter, which focuses on the electrical characterisation of the devices fabricated within this work.

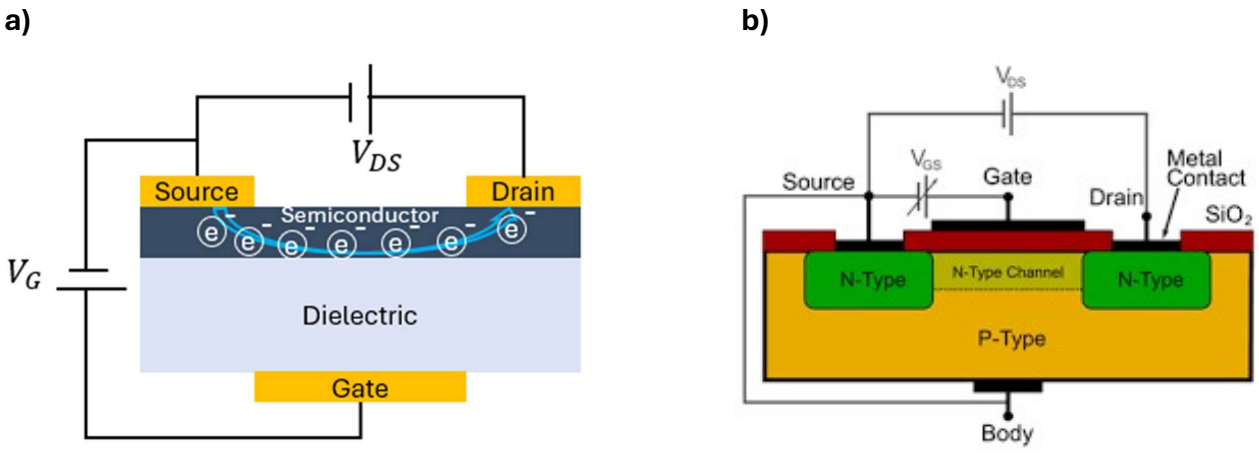


Figure 3 *a) The TFT device operation. A representative structure of n-channel (electron-transporting) TFT. The gate voltage (V_{GS}) induces charge accumulation at the interface between semiconducting and dielectric layers, and these accumulated charge carriers are swept by the applied source-drain bias (V_{DS}). b) Schematic of an n-channel MOSFET. The gate voltage (V_{GS}) controls the formation of a conductive channel between the source and drain. When V_{GS} exceeds the threshold voltage, an inversion layer forms in the p-type substrate, allowing current I_{DS} to flow.*

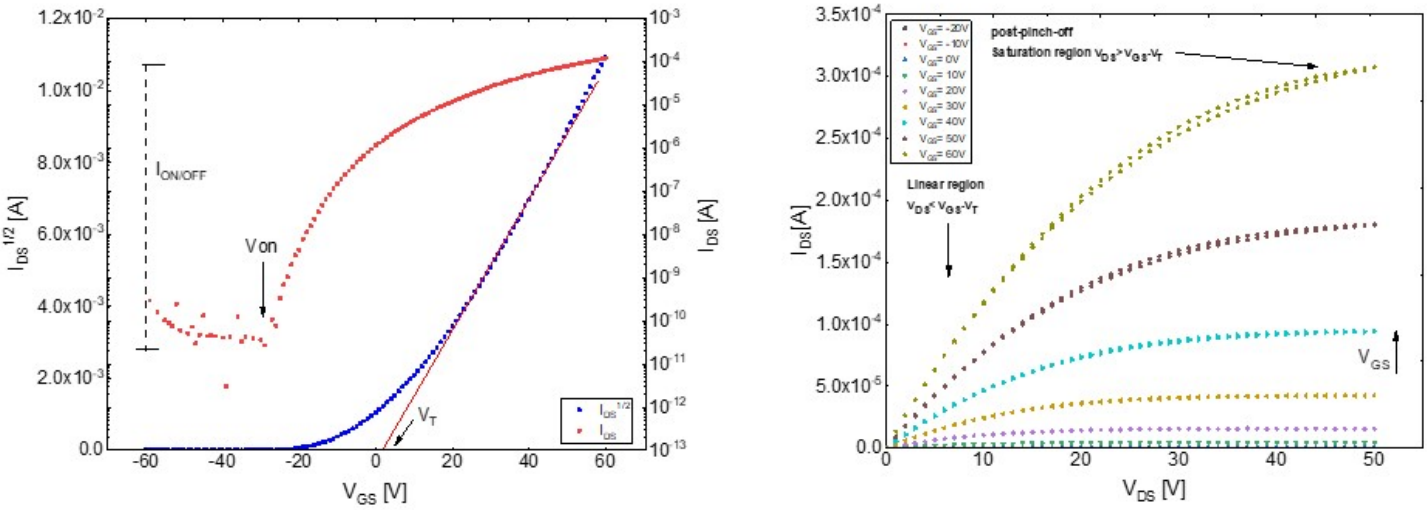


Figure 4.*a) Transfer characteristic, showing the square root of the drain current ($I_{DS}^{1/2}$, left y-axis) (blue) and the absolute drain current (I_{DS} right y-axis) in logarithmic scale (red) as a function of the gate-source voltage (V_{GS}). The gate voltage (V_{GS}) is swept from -60V to 60V. The threshold voltage (V_T) obtained through a linear fit (red straight line) to the $I_{DS}^{1/2}$ curve, as indicated in the plot. The turn-on voltage (Von) and the ON/OFF current ratio ($I_{ON/OFF}$) are also marked. b) Output characteristic. The different curves, distinguished by colour, represent the output characteristics for varying input conditions, with each colour corresponding to a different input voltage as indicated in the legend. Gate voltage (V_{GS}) ranged at $-20 \leq V_{GS} \leq 60$ V over output measurements, with a step of 10 V.*

Field-effect mobility

TFT field-effect mobility indicates its conductivity over the threshold. This property is linked to carrier movement in the sample, which directly influences the device's maximum I_{DS} and operating frequency.[15] Several methods are used for extracting the mobility values.[8]

Field-effect mobility quantifies how efficiently charge carriers move through a TFT's semiconductor channel when an electric field is applied. The importance of mobility in TFT stems from the fact that the higher the mobility, the greater the source–drain current (I_{DS}), within a certain span of the gate voltage (V_{GS}), at a given source–drain voltage (V_{DS}). The values for the linear mobility, μ_{lin} (also known as field-effect mobility, μ_{FE}), and saturation mobility, μ_{sat}, can be obtained from the transfer curve.[10]

Specifically, when $V_{DS} \ll (V_G - V_T)$, where V_T is the threshold voltage, the device operates in the linear regime. In this state, I_{DS} is approximately proportional to V_{DS}, and charge accumulation across the channel is relatively uniform. For the linear regime, the mobility is extracted from Equation 1:

$$I_{DS} = \frac{\mu C_{ox} W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] \quad (1)$$

Where μ is the field-effect mobility, L is the channel length, W is the channel width, C_{ox} is the gate oxide capacitance per unit area, V_{GS} is the gate-source voltage, V_{DS} is the source-drain voltage, and V_T is the threshold voltage. [1, 3, 9]

When $V_{DS} \geq (V_{GS} - V_T)$, the device operates in the saturation regime. In this condition, the conducting channel is pinched off at the drain end due to the high V_{DS}. Under these bias conditions, the current in the transistor channel becomes independent of V_{DS} , and I_{DS} reaches a constant value. For the saturation regime, the mobility is extracted from Equation 2:

$$I_{DS} = \frac{\mu C_{ox} W}{2L} (V_{GS} - V_T)^2 \quad (2)$$

Mobility, μ, is influenced by factors like the choice of semiconductor material, temperature, and various scattering mechanisms, such as lattice vibrations, ionized impurities from dopants, grain boundaries in polycrystalline materials, velocity saturation effects, and interface states or traps from structural defects.[15,16] Generally, higher mobility values support faster switching speeds, improved load-driving capacity, and enhanced accuracy in signal transmission.[4]

On/off current ratio

TFTs are electronic components used to regulate the current flow in electronic circuits. The on-to-off current ratio is one of the most important parameters for evaluating their functionality. The on-off ratio, $I_{ON/OFF}$, is the maximum to minimum I_{DS}, defined in a transfer curve. The minimum I_{DS} is usually given by the noise level of the measurement, while the maximum I_{DS} depends on the semiconductor material properties, as well as on the effectiveness of capacitive injection by the field effect.[1] The on-state corresponds to the current flow when the transistor is activated, whereas the off-state corresponds to the current level when the transistor is deactivated. The on-to-off current ratio determines the transistor's ability to switch between these two states. [7, 3]

Threshold and ON Voltage

In a TFT, V_T is an important parameter that determines the V_{GS} required to activate the device and induce current flow in the channel. The V_T is the V_{GS} at which the device switches from off to on, or when it starts to conduct current. In practice, the V_T of a TFT can be determined empirically by observing the device's properties at various V_{GS}. A typical approach is to plot the device's transfer characteristics, which demonstrates the relationship between the I_{DS} and V_{GS} for a given V_{DS}. V_T is often referred to as the V_{GS} at which the slope of the transfer curve changes significantly, indicating a transition from the off to the on state. Other variables that can be influenced by the V_T include the thickness of the channel layer, the work function of the gate electrode, and the character of the gate dielectric.[1] Despite the large number of published work in which the threshold voltage, V_T, is used as a parameter of study in TFT

analysis, the possibility of incorrect estimation should always be noted. This lies on the V_T estimate routine, which includes extrapolating the linear region of a typical transfer curve. The concept of V_{ON} is often used in literature, and it simply refers to the V_{GS} at which I_{DS} starts increasing or in other words, the V_{GS} required to fully turn on the transistor.[3, 9] A more detailed discussion of the extraction of the threshold voltage from the transfer characteristic are discussed in a subsequent chapter.

Subthreshold voltage swing

The subthreshold swing, SS, is an important performance parameter for TFTs, particularly in low-power applications. It measures the TFT's sensitivity to changes in the V_{GS}, which indicates the device's ability to turn on and off efficiently. The subthreshold swing represents the V_{GS} change required to change the subthreshold current by a factor of 10 and corresponds to the slope of the I_{DS} log versus the V_{GS} in the subthreshold region of the transfer characteristics plot. A smaller subthreshold swing is preferable for TFTs because it indicates higher switching efficiency and lower power consumption. This statement is true because a smaller subthreshold swing allows the TFT to turn on and off more efficiently, requiring a smaller voltage swing to drive the device between these two states. As a result, a smaller subthreshold swing reduces the device's power consumption and enables faster switching speeds.[1, 3] Subthreshold swing is usually expressed in millivolts per decade (mV per dec), representing the steepness of the I_{DS}–V_{GS} curve on a logarithmic scale. A lower value implies a higher sensitivity and efficiency of the transistor, as it requires less V_{GS} to switch between on and off states. This point will be addressed when the experimental results are discussed. This value is calculated using the following Equation 3:

$$S = \left(\frac{d log(I_{DS})}{dV_{GS}} \Big|_{max} \right)^{-1} \quad (3)$$

2.2. Metal Oxides

2.2.1. Introduction to Metal Oxides

The existing thin film technology is largely dominated by traditional silicon (Si) microchip-based electronics that rely on conventional vacuum-based processing methods. However, the economic and technological limitations of Si technology such as restricted charge carrier mobility, high production costs, and incompatibility with flexible substrates necessitate a significant shift in both material selection and manufacturing techniques.[7, 11,12] Additionally, the growing demand for large-area, flexible, and low-cost electronics for unconventional displays, wearable and ultralight devices, and disposable circuits necessitates the development of advanced electronic materials and cost-effective fabrication processes.[13-15] Researchers have investigated metal oxides (MOs) as an alternative to crystalline silicon and other III-V semiconductors due to their distinctive properties. These include high carrier mobilities, even in the amorphous state, resistance to mechanical stress, compatibility with organic dielectric and photoactive materials, and high

optical transparency. Additionally, electronic-grade MO thin films of high quality can be produced using vapor- and solution-based methods under near-ambient conditions (~25 °C in air), making them suitable for a wide range of applications such as cost-effective circuits, flexible OLED displays, and solar cells on plastic substrates.[16] In comparison to amorphous hydrogenated silicon and organic semiconductors, metal oxide semiconductors provide enhanced electrical, optical, chemical, and mechanical properties for thin-film transistors. These materials feature wide bandgaps, high mobilities, large current densities, very low off currents, and high optical transmittance in the visible spectrum. They also exhibit good environmental stability and are compatible with low-cost, vacuum-free large-area manufacturing techniques, all of which can be achieved at relatively low processing temperatures.[5] Over the past few decades, silicon-based transistor technology has dominated the electronics industry due to its excellent electrical properties and scaling capabilities; however, its fabrication process limitations have hindered large-scale production and integration on flexible substrates. Thin-film transistors have been extensively developed, with significant implications for large-area electronics. TFTs offer manufacturing benefits, allowing them to be produced on various substrates, including flexible plastics, skin, and even textiles. Various TFTs are being investigated for applications in flexible displays, biosensors, and healthcare electronics.[17] The semiconductor material determines the type of operation (p-type or n-type) in the transistor, with p-type TFTs function under a negative gate-source voltage bias using p-type semiconductors, and n-type operate with a positive gate-source voltage bias using n-type semiconductors.[18] To tackle the limitations of current thin film technology and address these challenges, metal oxides (MOs) [19, 20] have emerged as a promising alternative due to their excellent electrical and optical properties, such as high charge carrier mobility, transparency,[16] and mechanical stability. Moreover, they have attracted significant interest for electronic applications due to their adjustable structures, distinctive properties, and easy processing techniques. MOs are classified as semiconductors or insulators based on the differences in band position and bandgap.[21] Their integration into low-dimensional metal oxide heterostructures has been shown to result in mobilities that rival those of poly-Si. Furthermore, MOs have a unique processing versatility because they may be generated using both vapor- and solution-phase processes.[22 -24] Their supremacy will be reinforced as they pioneer a new industrial route in electronics, characterised by up-scaling and high-throughput manufacturing.[25,26] The strength of metal oxides lies in their diverse optoelectronic properties, which influence energy level alignment and ultimately impact the performance of electronic devices. Most MOs are semiconductors and are categorized into n-type materials, such as tin oxide (SnO_2), indium oxide (In_2O_3), zinc oxide (ZnO), and titanium dioxide (TiO_2), and p-type materials, such as nickel oxide (NiO) and copper oxide (CuO). Most MO semiconductors exhibit n-type behaviour. However, the significance of p type oxides is growing due to their critical role in the production of complementary logic circuits. NiO was the first p-type oxide ever identified in 1993.[27] Combining different MO materials can result in a variety of nanojunctions, including n-p, n-n, and p-p junctions. These combinations produce various structures and attributes that must be investigated separately to improve performance.[19] Metal oxide materials have also emerged as a promising platform due to their excellent performance as transparent electrodes, high-mobility semiconductors, and high-k dielectrics.[13] Although

these materials surpass conventional semiconductors in many aspects, their optoelectronic properties are highly dependent on their crystal structure, which is defined by the deposition technique and conditions.

2.2.2. Properties of Metal Oxide Semiconductors

Metal oxide semiconductors (MOS) have typically been produced using vacuum-based deposition techniques such as sputtering, pulsed laser deposition, chemical vapor deposition, atomic layer deposition, and ion-assisted deposition. These methods have enabled the fabrication of a broad range of MOS materials with high carrier mobility and low carrier concentration, making them suitable for use in thin-film electronics. Solution-processed deposition methods offer several benefits. Additionally, various solution-processed printing techniques allow for direct patterning, potentially serving as an alternative to traditional photolithography.[28] Metal oxide semiconductors differ significantly from traditional inorganic semiconductors like silicon and III-V compounds in terms of material design principles, electronic structure, charge transport mechanisms, defect states, thin-film processing, and optoelectronic properties. These differences enable both conventional functionalities and novel applications. Recent advancements in metal oxide semiconductors have been notable, including the discovery and characterisation of new transparent conducting oxides, the development of p-type MOS alongside the more common n-type for transistors, p-n junctions, and complementary circuits, formulations for printing metal oxide electronics.[16] The formation energy of native acceptors is greater than that of native donors, such as oxygen vacancies, which restricts the generation of holes. Moreover, the significant localization of the valence band maximum to oxygen ions leads to a high hole effective mass and low mobility. Consequently, most metal oxide semiconductors are n-type materials, and even p-type metal oxides like CuO, SnO, and NiO display low charge mobility.[18] While solution processing can produce high-quality films at a relatively low cost, the performance of pristine MOS films may be limited due to oxygen-related defects in the active layer, such as hydroxyl groups and oxygen vacancies, which introduce deep trap states within the band gap.

Metal oxide semiconductors, featuring tunable bandgap values ranging from 1 to 3 eV and high carrier concentrations ($N > 10^{19}$),[21] are promising transparent channel materials that have attracted significant attention in the microelectronics industry.[21, 30] Many MOS have energy gaps greater than 3 eV, hence, they are transparent in the visible spectrum. MOS have recently gained popularity as channel layers for TFTs in display devices due to their outstanding electrical properties, including high charge density, good optical transparency, ease of processing, stability, low cost and large-area electrical uniformity and mechanical flexibility. Currently, indium oxide and two or three component mixed oxides including indium, such as indium zinc oxide or indium gallium zinc oxide, have been shown to be high performance, solution-preparable metal oxide semiconductors with good light transmission within the visible range.[29] Remarkably, the performance of TFTs made through the simple solution process has approached the levels achieved by traditional vacuum-based methods.[10]

2.2.3. Properties of Indium Oxide

Indium oxide (In_2O_3), zinc oxide (ZnO), and tin oxide (SnO_2) are among the most frequently used metal oxide semiconductors. Materials with lower mobility values (relative to single crystalline Si with $\mu > 400$ cm^2/vs) are often degenerately doped to achieve high σ values.[7] Moreover, these materials are becoming attractive due to high transparency, low-temperature processing, and potentially better device performance and stability compared with the amorphous silicon and organic counterparts.[31] A significant advantage of using single component In_2O_3 is that high-performance TFT films can be produced through an aqueous route, eliminating the need for organic additives in the solution preparation. This strategy reduces costs and eliminates environmental effect, making In_2O_3 an attractive option for future high-performance display displays.[29] Indium oxide is an n-type semiconductor with a direct band gap of 3.5-3.7 eV and an indirect band gap of approximately 2.6 eV.[32] The n-type conductivity of In_2O_3 arises from deviations in its stoichiometric composition, with excess indium atoms or oxygen vacancies acting as electron donors. The material properties of indium oxide mentioned in the literature often range significantly from one another due to varied fabrication methods and oxidation states of the samples. Recently, low-dimensional and nanostructured semiconducting oxides such as ZnO, CdO, and In_2O_3 [33] have gained significant attention for their unique properties compared to thin films, as well as their potential applications in nanoelectronics, photonics, and sensor technology.[32] Thermal annealing is a commonly used technique to enhance crystal quality, examine structural defects, activate dopants, and form ohmic contacts in semiconductors. During annealing, structural defects like dislocations move within the material, and adsorption or decomposition occurs on the surface, altering the material's structure and stoichiometric composition. Several fabrication methods for In_2O_3 have been thoroughly explored, including evaporation, sol-gel processing, spray pyrolysis, sputtering, chemical vapor deposition (CVD), and atomic layer deposition (ALD). Among these, physical vapor deposition (PVD) techniques like evaporation and sputtering are commonly used in commercial applications to produce In_2O_3 thin films.[34] As a potential channel material, indium oxide has been extensively researched due to its ability to provide high electron mobility derived from the ns orbital of indium. Additionally, In_2O_3 is one of the semiconductor materials that can be synthesized through a solution process, exhibiting varying electrical performance based on its stoichiometry and the presence of defects within the material. By combining the benefits of the "aqueous route" with In_2O_3, aqueous In_2O_3 emerges as an excellent candidate for creating high-mobility channel layers in thin-film transistor devices at low temperatures.[35] Additionally, the gate dielectric is crucial in influencing the electrical performance of oxide thin-film transistors. Typically, gate dielectrics need to be smooth, dense, and free of pinholes to ensure low leakage currents and a high breakdown electric field.[36] However, for metal oxide dielectrics fabricated at low temperature (< 300 °C), it is difficult to achieve the purposes. Materials like indium oxide and tin oxide possess a wide energy bandgap (Eg > 3.4 eV) and are therefore transparent in the wavelength region from about 350 to 800 nm, where the long wavelength cutoff depends on the charge carrier concentration. [37] Although we focus here on metal oxide semiconductors, metal oxides with more conducting or insulating character can also be implemented in every TFT component,

including the gate, source and drain electrodes, and the gate dielectrics. In this work indium oxide films were used as the semiconductor layers in the TFTs. The experimental setup will be described in a subsequent chapter.

2.2.4. Role of dielectric layers in thin-film transistors

Dielectric materials are electrical insulators that become polarized when subjected to an electric field. Instead of allowing free electrical carriers to move through them, these materials experience a slight shift in the distribution of charges from their equilibrium positions, leading to dielectric polarization. This polarization is typically due to charge redistribution, which weakens the external electric field. The choice of dielectric materials for such devices must be carefully studied, particularly in terms of performance within a suitable frequency range.[17] Gate dielectric insulator is one of the essential and primary components of TFT, which plays a key role in high performance device. When gate potential is applied across the dielectric thin film, electrical charges of such dielectric material shift from their average equilibrium position, causing the dielectric polarization.[2] In a typical TFT structure, the dielectric layer is positioned between the gate electrode and the semiconductor. The gate bias induces polarization in the dielectric layer, which modulates the charge flow through the semiconductor channel between the source and drain electrodes. Several key requirements[38] apply to both the dielectric layer and its interface with the semiconductor: (1) reduced film thickness and a high dielectric constant to achieve high areal capacitance, which reduces power consumption (2) high film density to minimize leakage current (3) minimizing defects such as dangling bonds and interstitial/substitutional defects that hinder effective polarization and (4) a smooth surface morphology and good surface energy compatibility between the dielectric and semiconductor layers, which promotes charge accumulation, reduces charge-trapping sites at interfaces, and enhances charge carrier mobility for improved TFT performance.

2.3. Fabrication methods

Metal oxide thin films can be produced using a variety of manufacturing methods, which are broadly divided into two categories: physical and chemical-based processes. Sputtering, physical vapor deposition, and electron beam evaporation are common physical processes. These methods use physical processes to produce thin layers of metal oxides on substrates, typically in vacuum conditions. Chemical methods, on the other hand, use carefully regulated chemical reactions to create the suitable thin films. Sol-gel chemistry is a technique that involves the synthesis of metal oxide precursors, that undergo a series of reactions to create thin films after deposition. Chemical vapor deposition (CVD) and atomic layer deposition (ALD) are advanced technologies that involve gaseous reactants interacting with surfaces to build thin, homogeneous layers.[47] More precisely, metal oxides films can be deposited using vapor- and solution- phase techniques as summarized below.

i) Vapor-phase processing. There are four main vapor-phase techniques for depositing MO films: Thermal deposition, sputtering, pulsed laser deposition and atomic layer deposition.

ii) Solution-phase processing. There are three main solution-phase techniques for depositing MO films: Spin-coating, spray coating and printing.

Conventional vapor-phase deposition technologies create high-quality metal-oxide thin films for many applications, but they confront intrinsic limitations in large-area deposition, which is important for "macroelectronics". Such devices require use of substrates that are far larger than semiconductor production facilities can currently handle. As a result, solution processing provides opportunities for growth in the macroelectronic technology sectors. Solution processing has several advantages over vapor-phase deposition, including possibly reduced costs, ambient processing conditions, high throughput, roll-to-roll capability, simple composition tuning, and the use of ecologically benign solvents/precursors.[48, 49] Despite these advantages, solution-processed metal oxides frequently contain more impurities/defects than vapor-deposited films, resulting in less desirable characteristics. However, tremendous progress has been made over the last decade, enabling the creation of solution-processed metal-oxide thin films with high (opto)electronic quality competitive with vacuum-deposited films.[22] Increased knowledge of how the chemistry of the solution-precursor influences the ensuing thin-film materials' structure and morphology, which in turn affects their function, has contributed to these advancements. Such relationships are well-established for films prepared from sol–gel precursors.[47] There are two types of solution deposition processes: entire-area deposition and selective-area deposition. For entire-area deposition, chemical bath deposition, spin coating, and dip coating are typically utilized, while printing techniques are employed for selective-area deposition. Conventionally, the entire-area deposition method, such as spin-coating, is used mainly because the resulting oxide TFTs exhibit high performance and reliability, compared with their printed counterparts. In this work the spin coating method was used. A deeper analysis of this method is presented in a subsequent chapter. Nonetheless, selective-area deposition has grown in significance as printing techniques have been used more often in recent years because of its reduced material requirements, affordability, environmentally friendly processing, and improved device performance.[23]

2.4. History of Metal Oxide TFTs

Conventional fabrication methods for oxide semiconductor devices typically involve many photolithographic steps and vacuum-deposition processes. However, solution-processes are very attractive because they provide a novel cost-cutting method while expanding the substrate size, lowering the number of mask phases, and eventually enhancing the manufacturing yield. Over the last 50 years, sol-gel technologies have been extensively studied as a low-temperature alternative for producing MOs, ceramics, and glasses. A sol-gel system is a solution in which various polymerization and polycondensation processes result in the creation of a solid phase network.[50] Recent results of solution processed oxide TFTs are summarized below.

Ohya et al.[51] in 2001 developed a ZnO thin film on a Si wafer with an oxidized SiO_2 layer using a chemical solution deposition procedure, and it was used to a bottom-gate type thin film transistor. Norris, et al.[52] demonstrated a ZnO transparent thin-film transistor with a channel layer created by spin-coating deposition. Spin-coated ZnO nanocrystals films used by Sun

et al. to fabricate high-performance TFT devices at low temperatures.[53] In 2006, Cheng et al. [54] decided on a ZnO film patterning process and built a bottom-gate type TFT device with a patterned active channel ZnO film using the chemical bath deposition method. In 2007, Ong et al. [55] announced a method for producing a solution-processed high-mobility ZnO thin-film semiconductor by thermally treating a solution-fabricated ZnO precursor film at moderate temperatures. Chang et al. [56] also reported this year on a simple and cost-effective method for spin coating extremely transparent amorphous zinc tin oxide thin films in ambient conditions A simple, low-cost and nontoxic aqueous ink chemistry was suggested for digital printing of ZnO films. High-quality, polycrystalline ZnO films were deposited by ink-jet printing and spin-coating.[57] The performance of TTFTs with an amorphous IZO active layer was also reported by Choi et al. [58] in 2008. The amorphous IZO semiconductor thin films were fabricated by solution process in ambient air conditions using metal acetates as precursors. Kim et al. [59] also in 2008 reported the first demonstration of solution-processed In_2O_3 TFTs using SiO_2 and self-assembled nanodielectric as gate dielectrics. Kim et al. [60] in 2009 proposed the study of the chemical reactions in the IGZO solution with varying indium content and explained the structural and electrical properties of sol-gel derived IGZO films. Thin-film transistors based on inkjet printed indium zinc tin oxide (IZTO) channel layers reported in 2009 by Lee et al. [61] This year Hwang et al. [62] also fabricated thin-film transistors with aluminum indium oxide channel layers via a simple solution process. Sol–gel processed and lithographically patterned amorphous zinc–tin oxide (a-ZTO) thin-film transistors with high mobility and good stability were demonstrated by Park et al. the same year. [63] Ryu et al. [64] in 2010 presented more extensive study results from earlier work on solution-processed amorphous IZO TFTs with excellent performance. Kim et al. [59] the same year presented the growth of amorphous ZITO-based TFTs in solution phase. Yang et al. [65] have created an active layer of indium-gallium-zinc-oxide (IGZO) nanoparticles made from a water solution in a bottom-gate thin-film transistor. Spin-coating was used to create polycrystallised $InGaZn_2O_5$ films. The following year, Banger et al. [66] reported the formation of amorphous metal oxide semiconducting thin films (a-IZO, a-IGZO) from soluble metal alkoxide precursors using a 'sol-gel on chip' hydrolysis approach. Kim et al. [67] in 2012 proposed a general method for producing high-performance and operationally stable metal-oxide semiconductors (IGZO) at room temperature using deep ultraviolet photochemical activation of sol-gel films. Hwan et al. [68] in 2013 proposed a novel aqueous method for producing indium-based (IZO) metal-oxide thin films as channel layers for TFT applications. The same year, Lin et al.[40] described the use of a solution-processable molecular ZnO hydrate precursor for the growth of ZnO films and high-performance transistors. These advancements highlight the continuous evolution of solution-based approaches for fabricating high-performance metal-oxide semiconductors, paving the way for further innovations in thin-film transistor technology.

2.5. Sol Gel Chemistry

2.5.1. Sol gel benefits

Sol-gel chemistry presents several advantages, primarily due to its ability to create solid-state materials from chemically uniform precursors. By capturing the "randomness of the solution state" and promoting atomic-level mixing of reagents, it enables the production of

complex inorganic materials, such as ternary and quaternary oxides, at lower processing temperatures and with shorter synthesis times.[7] Moreover, greater control over particle morphology and size should be possible using sol-gel chemistry. Since creating a homogenous precursor at room temperature does not guarantee homogeneity throughout a reaction and many sol–gel routes have therefore been designed to combat or control phase segregation during synthesis. It is not always essential to achieve complete "randomness" in the precursor. In fact, some of the most exciting recent developments in the sol-gel field have arisen from gels that exhibit a certain level of ordering and structure. One of the numerous advantages of this chemical processing approach is that it gives extraordinary control over the dimension, composition, and structure of the related films. This factor plays a crucial role in the advancement of various applications. Furthermore, recent advances in sol-gel technology have included alternate thermal treatment methods that use less energy to create thin films, making this approach substantially more cost-effective than previous physical procedures.[79] The sol gel method is also a well-known process for synthesizing metal oxide nanopowders due to its low temperature and low-cost process, using less amount of precursor material for preparing sol solution, can be evenly spread on the substrate, has a high purity process that leads to high homogeneity, can synthesize highly volatile substances, has a high melting temperature, and can produce a variety of structures.[46] As mentioned above sol-gel processing has several advantages for optical and electronic applications, including: (i) ambient temperature for sol preparation and gel processing; (ii) product homogeneity; (iii) low sintering temperature; (iv) ease of making multi-component materials and (v) good control over powder particle size, shape, and size distribution.[80]

2.5.2. Sol gel development

Recently, significant research has focused on developing cost-effective methods for producing high-quality oxide electronic materials, considering factors such as raw material costs, processing time and complexity, and reliability. In general, sol–gel method can be described in five key steps: hydrolysis, polycondensation, aging, drying and thermal decomposition.[79] Sol–gel methods are particularly attractive for their compatibility with printing processes for the fabrication of metal oxide TFTs and other optoelectronic devices. Solution-based deposition has emerged as one of the most promising techniques, as it enables the production of large-area metal oxide layers with low material and processing costs. The concept of "ceramics from solution" was first introduced by Ebelmen over 150 years ago when he proposed sol-gel technology to synthesize silica-based materials using silicon alkoxide precursors. However, it was only within the last decade that sol-gel technology has seen significant advancements, expanding its use in a variety of applications using functional metal oxide materials.[81] A sequence of processes including gelling, pressing, drawing, and casting are applied to the produced solution, causing different structural and phase alterations. This enables the creation of bulk monolithic products, fibres, coatings, powders etc. A sol-gel system is a solution in which a solid phase network is formed as a result of polymerization and polycondensation processes.[82] Sol-gel chemistry involves transforming liquid precursors into a colloidal suspension (sol) and then a network structure (gel). Sol-gel metal oxide research has made significant progress over the last

decade.[22] Sol-gel chemistry involves the preparation of inorganic polymers or ceramics from a solution, transitioning from liquid precursors to a sol and ultimately forming a network structure known as a "gel." The formation of a sol occurs through hydrolysis and condensation of metal alkoxide precursors. However, a sol is more broadly defined as a colloidal suspension, which applies to a wider variety of systems beyond just metal alkoxides (Figure 5). [83, 38] In this work, the sol gel method was used to fabricate the semiconductor layer of the thin film transistors.

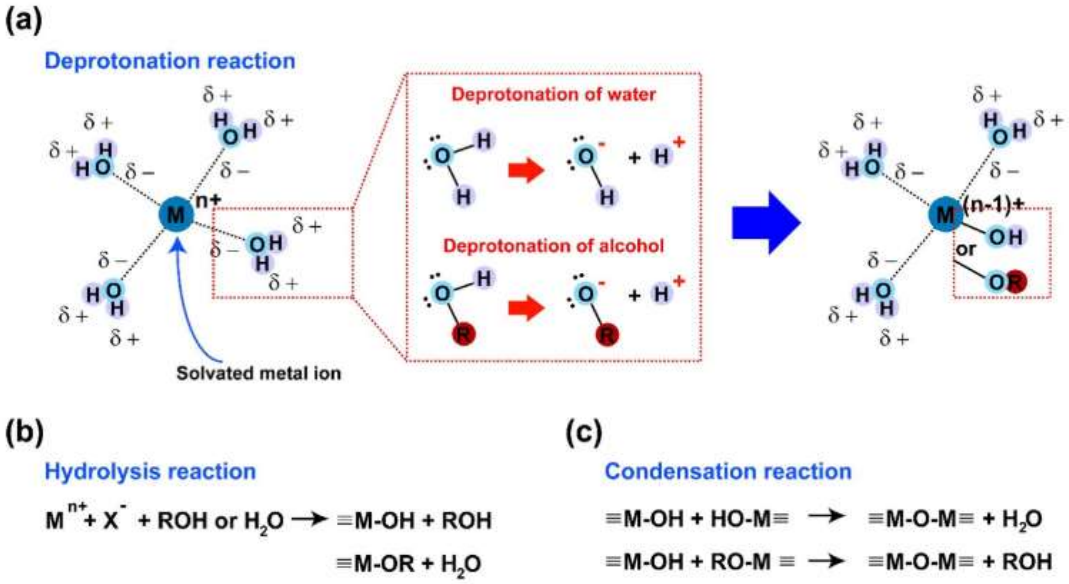


Figure 5. *Sol-gel chemistry in metal oxide materials. a) A schematic of reaction between metal ions and water/alcohol molecules to metal hydroxides. After water or alcohol molecules are deprotonated, metal and hydroxide ions are bound to each other by electrostatic interaction. Representative chemical reactions are shown for b) hydrolysis and c) condensation.*

The steps leading to MO thin film formation based on sol-gel chemistry are discussed below.[79]

Step 1: Synthesis of the sol: This involves hydrolysis and partial condensation of alkoxides to form the initial sol. The creation of metal oxide requires oxygen, which can be obtained from water or organic solvents. The aqueous sol-gel method uses water as the reaction medium, whereas the nonaqueous sol-gel procedure uses organic solvents as the reaction medium. In addition to water and alcohol, an acid or base can aid in the hydrolysis of the precursors. The general chemical reaction for the hydrolysis process is as follows:

M-OR +H_2O → MOH + ROH (Hydrolysis)

where M= Metal, R=Alkyl Group (C_nH_{2n+1})

The solvent molecules (e.g., H_2O or ROH) solvating metal cations are transformed into hydroxo (OH^-) or oxo (O_2^-) ligands, leading to metal hydroxides. The amount of water has a substantial influence on gel formation; a higher water content promotes the creation of a

higher ratio of bridging to nonbridging oxygens, resulting in a more polymerised and branched structure during condensation.

Step 2: Gel formation: Polycondensation reactions lead to the formation of a gel network, creating metal–oxo–metal or metal–hydroxy–metal bonds. This step involves the condensation of adjacent molecules, during which water or alcohol is eliminated, and metal-oxide linkages are formed. This leads to the growth of polymeric networks to colloidal dimensions in the liquid state. Condensation occurs through two mechanisms: **olation** and **oxolation**. The kinetics of olation are rapid compared to oxolation.

- **Olation** refers to the formation of a hydroxyl (–OH) bridge between two metal centres, resulting in metal–hydroxy–metal bonds. Olation corresponds to the nucleophilic addition of a negatively charged OH group onto a positively charged hydrated metal cation.
- **Oxolation** involves the creation of an oxo (–O–) bridge between two metal centres, forming metal–oxo–metal bonds. This reaction could be described as the dehydration of olated species via the formation of one water molecule between two hydrogen bonded OH groups. It is catalysed by acids which favour the protonation of the leaving water molecule.[84]

The general chemical reaction for the condensation process can be represented as:

M-OH +XO-M → M-O-M + XOH (Condensation)

where M= Metal, X=H or Alkyl Group (C_nH_{2n+1})

Condensation, or polycondensation, leads to an increase in the viscosity of the solvent, resulting in the formation of a porous structure that retains its liquid phase, known as a gel. The oxide thin film is formed by coating the precursor solution and subjecting it to a post-annealing process, usually above 400 °C, to (1) facilitate M−O−M structure formation (condensation), (2) remove byproducts and solvents through evaporation/decomposition (impurity removal), and (3) densify the resultant oxide film through void removal.[22] Hydrolysis and condensation chemistry is constrained by the limited number of elements that easily form alkoxides, as well as the high reactivity of many of these compounds.[83]

Step 3: Syneresis (or aging): Further condensation occurs within the gel network, often causing it to shrink and expel solvent. The aging process causes continuous changes in the structure and properties of the gel. During the aging process, polycondensation continues inside the confined solution, as does reprecipitation of the gel network, resulting in decreased porosity and increased thickness between colloidal particles.

Step 4: Drying the gel: This can result in a dense xerogel, formed by the collapse of the porous network, or an aerogel, achieved through supercritical drying. The drying process is complex because water and organic components separate to produce gel, disrupting its structure. There are three types of drying processes: atmospheric/thermal drying, supercritical drying, and freeze-drying, each of which has a different effect on the structure of the gel network.

Metal nitrates, M(NO_3) x, have proven to be more effective than other commonly used salt precursors for metal-oxide films. Films produced from metal nitrates are generally denser, contain fewer impurities, and require lower processing temperatures due to the high volatility of their decomposition byproducts. As a result, these thin films often exhibit excellent electronic properties in solution-processed materials and have been used in various applications, including semiconductors, dielectrics, transparent conducting oxides (TCOs), magnets, solid electrolytes, and charge-carrier selective contacts. Nitrate counterions have distinct reactivities, making them susceptible to breakdown pathways that require little to no thermal annealing. These "low-temperature processing" techniques, such as combustion synthesis, ultraviolet photolysis, and water-vapor annealing, have been explored for thin film processing to enhance compatibility with low-melting-point polymer substrates and facilitate roll-to-roll manufacturing.[85, 86] While metal-nitrate precursors are widely used, a fundamental understanding of nitrate decomposition pathways and oxide formation processes is essential for the advancement of thin film solution-deposition technologies.[47] In Figure 6 are presented the fabrication steps of sol-gel metal oxide films.[7]

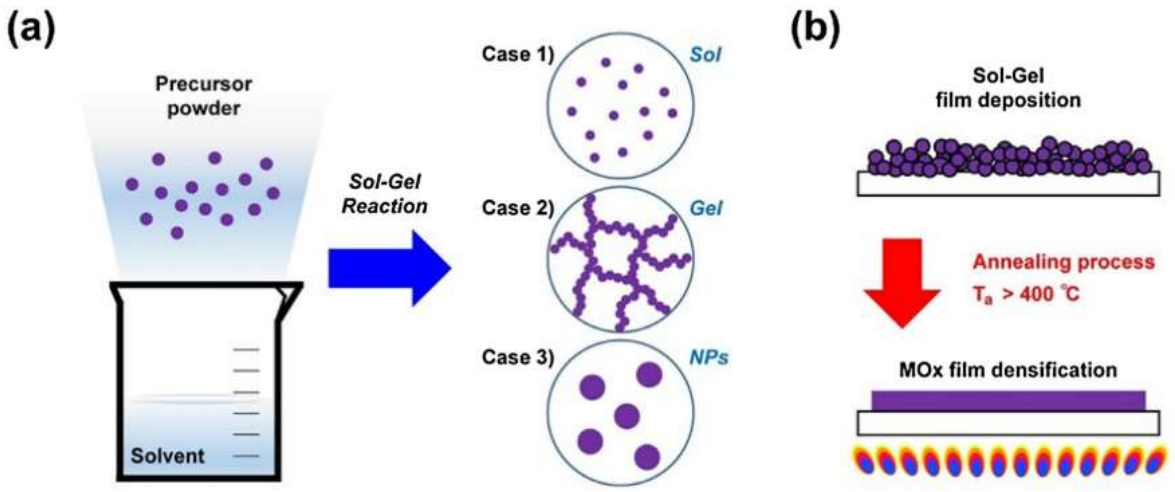


Figure 6. *Fabrication of sol-gel metal oxide films. a) Typical sol-gel metal oxide reaction products (i.e., sol, gel, and nanoparticles) depending on reaction parameters such as temperature, duration, pH, and catalyst. b) A schematic of densifying a sol-gel MO film from as-spun xerogel via high-temperature thermal annealing.*

2.5.3. Advances and challenges of Solution Processed Metal Oxide TFTs

In recent years, significant progress has been made in developing TFTs using various fabrication methods, such as chemical vapor deposition, sputtering, and spin coating from precursor solution. Importantly, TFTs fabricated using solution-based methods are easy to process and provide a low-cost, low-temperature approach to large-area coating, making them highly valuable for commercial applications.[23] The solution-processed oxide thin-film transistor is considered a promising next-generation device despite certain drawbacks

because of its many advantages, including easy composition adjustments, high throughput, eco-friendliness, simple manufacturing (photolithography is not needed for printing), cost-effective fabrication (using nonvacuum processing equipment and minimizing material waste through selective area deposition within the printing technique). Additionally, oxide TFTs offer significant advantages, including high mobility and particularly excellent uniformity, even on large-area substrates measuring 3 m × 3 m or larger.[23] From n-type semiconductors, the evolution of solution-processed metal-oxides has expanded into high-k MO dielectrics as well as p-type MO semiconductors, thus enabling the fabrication of TFTs solely based on solution processed layers, with device performances comparable to TFTs based on conventional technologies.[7] A recent trend in sol-gel metal oxide research is shifting from exploring different MO compositions with high electrical performance to creating innovative engineering methods that significantly lower the energy or temperature needed for post-deposition processing of high-quality sol-gel MO films. Recent advances in several types of solution-processed MO dielectric materials, large-area sol-gel oxide deposition, and low-temperature film production processes have been examined. Although significant progress has been made in the field of sol-gel MO dielectrics, several challenges remain concerning materials, processing methods, and device architectures and characterisation. It is essential to develop methods for controlling the crystallinity of sol-gel processed metal oxide materials, as well as techniques for characterizing the resulting TFT devices. This necessity arises from the fact that low-temperature processed oxide dielectrics may harbour significant defects or mobile charges, which can lead to ambiguous assessments of TFT performance. The detailed mechanism on the crystalline film formation from amorphous sol-gel oxide materials requires further investigation, which will be useful for finely adjusting other functionalities, such as ferroelectricity.[38] Additionally, in combination with rapid low-temperature oxide activation processes and surface chemical modification, the development of low-cost large-area sol-gel ink printing such as gravure and flexography are desired for the industry-scale fabrication of MO electronic devices and complex circuits. Finally, since dielectric materials are vital for low-power electronics by reducing leakage currents and lowering operational voltages, it is essential to develop suitable dielectric materials along with effective film deposition processes to satisfy these requirements. Despite the significant advancement in solution-based oxide semiconductors, there still exist several obstacles in terms of materials, processing, and device physics. First, the electronic structure of the solution-processed oxide semiconductors remains insufficiently understood. However, a complete understanding remains still unavailable. Second, for vacuum-deposited oxide TFTs, the device stability has been widely examined, since it is essential for practical display applications. However, the device stability manufactured using the solution process has not been thoroughly explored.[22] Moreover, despite all this progress, the demand for thermal annealing at high temperature still constitutes the biggest challenge. According to reported research, low temperature processing causes incomplete production of M-O-M networks, which are primarily replaced by M-OH. This substitution hinders carrier transport in metal-hydroxide lattices, resulting in a significant performance disparity between high- and low-temperature processed TFTs.[10] Therefore, to fully achieve all-solution-processed metal oxide flexible circuitry, it is crucial to develop a generalised methodology for the rapid conversion of as-

deposited xerogel-like oxide materials into high-quality thin films at low temperatures. This process should effectively eliminate metal ligands, condensation by-products, and other chemical impurities during the formation of M-O-M networks, utilizing various types of general metal oxide precursors.[13]

3. Experimental Methods

3.1. Thin Film Fabrication – Spin Coating

Spin coating is a straightforward method for creating thin films from solutions, with thicknesses ranging from nanometres to micrometres. This technique can be used with a variety of organic, inorganic, and composite materials. The process begins by applying the solution onto a flat substrate, which may be spun either before (dynamic) or after the solution is applied. The substrate is then rotated at a set speed, during which the solvent evaporates, resulting in the formation of a thin film. (Figure 7) [86] Key factors that influence the film's physical, electrical, and thermal properties include the solution's viscosity, surface energies of both the solution and substrate, spin speed, and duration.[87] Because the processes involved in thin film formation during deposition are well understood, spin coating remains one of the most widely used techniques for creating uniform layers in both academic research and industrial applications. The main reasons, for spin coating's universal application are high simplicity, uniformity, reproducibility, and compatibility regarding the use of different substrates. The principle of this technique is to achieve an equilibrium between the centrifugal force produced by a rotating stage and the viscous force caused by the solution's viscosity. When the solution is dropped onto the substrate, the rotating stage that holds the substrate is accelerated to high angular velocities, causing additional solution to be removed off the substrate's surface. The substrate is covered with the solution, and the spin coater quickly accelerates to a high rotational speed, which is maintained for a specified period. Once the spinning is finished, the thin film is formed because of both the liquid flow and solvent evaporation processes. It is important that the solution covers the substrate surface completely prior to the spinning. The thickness of oxide films produced by spin coating is influenced by factors such as the spinning speed, acceleration, steps, duration, number of repetitions, as well as the viscosity and molar concentration of the solution (Figure 8). Depending on the type of precursor used, the thin film may require some additional processing steps, such as heating or UV treatment, to be fully formed. Once the excess solution is removed, the film coatings undergo various drying and annealing processes. The modelling of spin coating processes is based on principles of fluid dynamics and surface interactions. By analysing various characteristics of a solution—such as viscosity, density, shear-thinning behaviour, and evaporation rates—a significant correlation between the parameters of spin coating and the resulting thickness of the deposited films has been established. The two primary forces that influence film thickness are liquid flow, which can be adjusted by modifying the acceleration and spin speed, and the evaporation of the precursor solution. For many materials, the impact of evaporation on thin film morphology is largely due to the faster evaporation rates compared to other types of solutions, especially aqueous ones.[50] Spin coating is arguably the most widely used

technique for solution-based deposition of oxide semiconductors. Its simplicity makes it ideal for research, allowing for rapid film deposition. However, it has limitations in terms of scalability, especially when producing large arrays of thin-film transistors.[88]

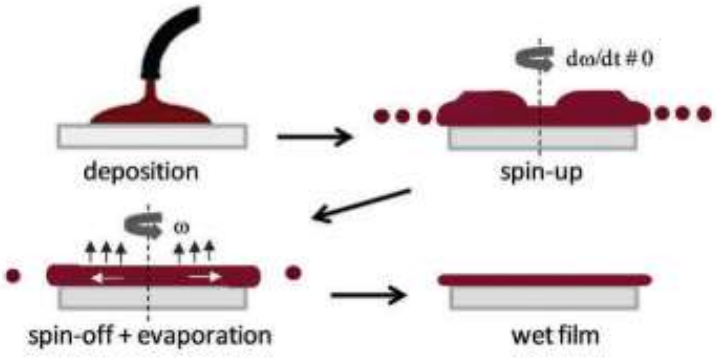


Figure 7. *Schematic representation of the spin coating process. The process begins with the deposition of the solution onto the substrate, followed by the spin-up stage, where the substrate rotates, spreading the solution due to centrifugal forces. During the spin-off and evaporation phase, excess solution is expelled, and solvent evaporation leads to film thinning. The process results in the formation of a uniform wet film on the substrate.*

Figure 8. *Spin coater used for thin film deposition*

Thickness equation

The thickness of a spin coated film is proportional to the inverse of the square root of spin speed as in the below equation where ω is angular velocity/spin speed and h_f is the final film thickness (Equation 4).

$$h_f \propto \frac{1}{\sqrt{\omega}} \quad (4)$$

The precise thickness of a film is influenced by the concentration of the material and the rate of solvent evaporation, which is affected by factors such as solvent viscosity, vapor pressure, temperature, and local humidity. Several efforts have been made to describe the spin coating process more rigorously. The earliest and most straightforward analysis was conducted by Emslie, Bonner, and Peck in 1958. This analysis made several assumptions, such as neglecting the effects of evaporation (which may be valid depending on the volatility of the solvent) and overlooking the potential for non-Newtonian behaviour.[89] As a result, it is assumed that the viscosity of the fluid remains constant and is not affected by stress (Equation 5).

$$\frac{\partial h}{\partial t} + \frac{\rho \omega^2 r}{\eta} h^2 \frac{\partial \mathrm{h}}{\partial \mathrm{r}} = -\frac{2\rho \omega^2 h^3}{3\eta} \quad (5)$$

t refers to the time elapsed since the process began, ω is the angular velocity, r is the distance from the centre of rotation, ρ represents the density, η denotes the viscosity, and h is the thickness of the fluid layer (as opposed to the dry thin film). The term ∂h / ∂t indicates the rate of change in thickness over time, while $\partial \mathrm{h}$ /$\partial \mathrm{r}$ describes the rate at which the fluid spreads radially.

If the film is considered initially uniform, this leads to a description of the fluid film thickness as seen in Equation 6.

$$h = \frac{h_0}{\left(1 + \frac{4\rho \omega^2}{3\eta} {h_0}^2 t\right)^{\frac{1}{2}}} \quad (6)$$

In this case, h_0 is the initial uniform thickness of the film at the beginning of the process. Since this model does not take evaporation into consideration, it cannot be used to determine the exact thickness of the final dry film. The first effort to incorporate the effects of evaporation was made by Meyerhofer in 1978,[90] who revised the equations originally developed by Emslie, Bonner, and Peck by adding a term for the solvent evaporation rate (Equation 7).

$$\frac{\partial h}{\partial t} = -\frac{2\rho \omega^2 h^3}{3\eta} - E \quad (7)$$

Here E is the uniform solvent evaporation rate, in units of solvent volume evaporated per unit area per unit time. Meyerhofer suggested that during the early stages of the spin coating process, the thinning of the film is primarily driven by fluid flow, while later, evaporation becomes the dominant factor (Equation 8). He also determined that if the shift from flow-driven thinning to evaporation-driven thinning happens suddenly, the film thickness can be calculated analytically. This calculation assumes that the film is thin enough for the solvent concentration to remain uniform throughout its depth.

$$E = \frac{(1 - C)\, 2\omega^2 \rho\, {h_0}^3}{3\eta} \quad (8)$$

Where C is the volume fraction of solute in the film and h_0 is the film thickness at the transition between the two film-thinning regimes. Then the final film thickness can be calculated using the Equation 9.

$$h_f = \left(\frac{3\eta_0\, E}{2(1 - C_0)\rho\omega^2}\right)^{\frac{1}{3}} \quad (9)$$

Where C_0 is the initial concentration of solute, and η_0 equates to $\eta(C_0)$.

The final thickness of a spin-coated film can also be estimated without accounting for the solvent evaporation rate (Equation 10). This is achieved by making several assumptions, such as assuming that the airflow remains laminar throughout the process.

$$h_f = \left(\frac{3}{2}\right)^{\frac{1}{3}} k^{\frac{1}{3}}\, C_0 (1 - C_0)^{-\frac{1}{3}} \rho^{-\frac{1}{3}} \eta_0^{\frac{1}{3}} \omega^{-\frac{1}{2}} \quad (10)$$

Spin coating duration

In most standard spin coating techniques, the goal is to keep the substrate spinning until the film is completely dry. This largely depends on the boiling point and vapor pressure of the solvent used, as well as the ambient conditions during the spin coating process. For most solvents, a spin coating duration of around 30 seconds is typically sufficient and is recommended as a good starting point for most procedures.

3.2. Aluminium Deposition via Electron Beam Evaporation

3.2.1. The Electron Beam Evaporation Process

Electron beam evaporation is a type of physical vapor deposition (PVD) technique where a focused electron beam is used in vacuum to heat the material for evaporation. The process relies on the emission of electrons from a tungsten filament when a current is applied. An electron beam system has two components – the electron gun, containing a filament, and the crucibles, containing the target materials for coating the substrate. The substrate is above the crucible in the vacuum chamber.[91] To generate the electron beam, the tungsten filament must be heated. An electron gun system generates an electric current of 5 to 10 kV through the tungsten filament, which is located outside the deposition zone. This high-voltage current heats the tungsten to temperatures that trigger thermionic electron emission. Permanent magnets are then used to direct the high-energy electrons towards the target material, which is placed in a water-cooled crucible. When the electron beam hits the crucible, the kinetic energy is converted into heat, causing the material to evaporate. The vapor then travels through the vacuum chamber and deposits as a thin layer on the substrate

via condensation. This method's precise, high-energy beam allows for the evaporation of materials with high melting points, which are difficult to evaporate using conventional techniques. Additionally, it enables high deposition rates at relatively low substrate temperatures. The deposition chamber is evacuated to a pressure of 10^{-5} Torr or lower. The target material is typically in the form of pellets. The deposition rate is influenced by both the starting material and the power of the electron beam. The thickness of the deposited film can be monitored in real-time using a quartz crystal monitor.[92] A schematic of the electron beam evaporation is presented in Figure 9.[93] Figure 10, below, shows the E-Beam evaporation equipment that was used in this work.

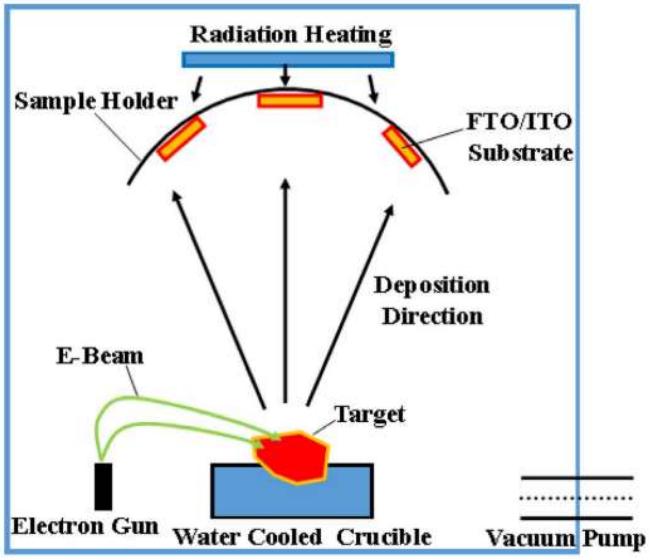


Figure 9. *Schematic of the electron beam evaporation process. An electron beam heats and evaporates the target material, which then condenses onto the FTO/ITO substrate under vacuum conditions.*

Figure 10. *E-beam evaporation equipment used for fabricating contacts*

3.3. Fabrication of Thin Film Transistors

Commercially available highly p-doped silicon (Si-p^{++}) wafers (resistivity: 0.001 - 0.005 Ωcm) with a thermally grown 200 nm thick layer of SiO_2 acting as gate and gate dielectric respectively, were used for the fabrication of bottom-gate, top-contact transistors (BG-TC). Prior to the deposition of the In_2O_3 layer, the substrates were cleaned by ultrasonication in deionized water, acetone, and isopropanol (IPA), with each step lasting 10 min. Between each step the substrates were dried under nitrogen (N_2). Substrates were subsequently exposed to atmospheric pressure UV ozone treatment for 30 min at room temperature, for wettability enhancement. The metal oxide precursor solution consisted of indium nitrate hydrate ($In(NO_3)_3{\cdot}H_2O$ and 2-methoxyethanol (2-ME) with a concentration of 30 mg/ml. The solution was stirred overnight at 50 °C, thus obtaining a clear form. The precursor solution was spin-coated after being filtered through a 0.22 μm syringe filter on the Si-p^{++}/SiO_2 substrates for 30 s at 4000 rpm, in an ambient environment. As-spun precursor layers were thermally stabilised by drying them on a hot-plate at 300 ^{O}C for 1 hour to remove excessive solvent residues. Finally, source and drain aluminum electrodes (100 nm thick) with an area of 0.015762 cm^{-2}, were deposited by e-beam evaporation via a shadow mask on top of the insulators. A back contact (gate) of 100 nm thick aluminum film was also deposited on the back of the silicon wafer (after removal of the native SiO_2 by scratching with a diamond tip pen). This way we achieved the fabrication of TFTs with a channel length (L) of 0.03 cm and width (W) of 0.15 cm. The device architecture of a bottom-gate top-contact thin-film transistor is shown in Figure 1.[16] Figure 11 presents the fabricated thin film transistors.

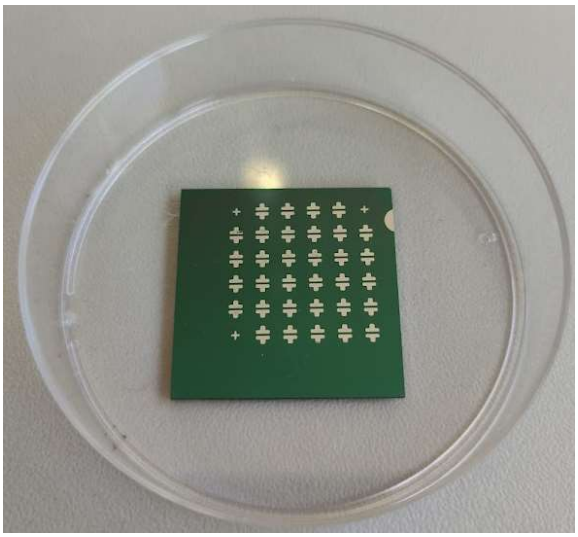


Figure 11. *This figure shows a representative fabricated thin film transistor array.*

3.4. Electrical characterisation - Equipment

In this work, the results are based on the electrical characterisation of thin film transistors. These measurements were performed on a setup including two SMUs (Source Measure Units) Keithley 2420 SMU and Keithley 6430 SMU as the principal measurement sources, along with a Semiprobe device measuring equipment. More specifically, the equipment includes the following:

Keithley 2420 and 6430: I-V measurements were performed using Keithley SMUs. The SMUs enabled precise control and simultaneous measurement of current and voltage, allowing for the accurate characterisation of the device's electrical properties (Figure 13(a)).

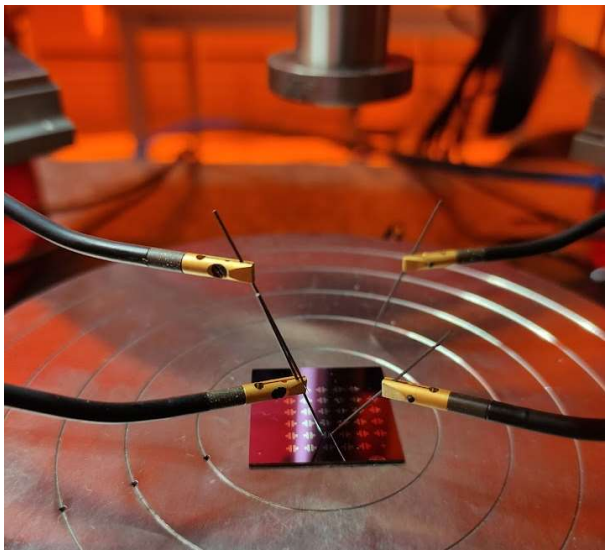
Semiprobe SMU probing table: The region where a device is positioned before measurement is designed to ensure precise probing of the sample. The table features a vacuum chuck to prevent any movement of the sample during testing. Probing arms, which are linked to Keithley 2420 and 6430 SMUs, are situated above the sample area, with probe tips attached to the ends of the probing arms (Figure 13(b)).

Microscope: Used in accurate device probing (Figure 13(c)).

PC: The I-V measurements were conducted using the software “Kickstart”, which was used to interface with the Keithley SMUs to automate and control the measurement process. Parameters such as voltage sweep ranges and measurement intervals were set through the software, and real-time data visualization was provided. This ensured that data collection was streamlined, and that precise.

a)

b)



c)

Figure 13. *a) Keithley 2420 and 6430 SMUs b) Semiprobe SMU probing table and microscope c) the sample with the probe tips attached to the ends of the probing arms*

4. Optical Reflectance Spectroscopy

4.1. Optical Reflectance Spectroscopy: Introduction and Measurements

Optical Reflectance Spectroscopy (ORS) was used to estimate the thickness of the dielectric and semiconducting layers of the TFT devices. It measures the intensity of light reflected off a material's surface when a specific amount of normally incident light is

directed at it. This reflectance measurement provides information about the material's surface properties and its interaction with light. It offers information on the sample's composition, properties and structure. ORS is a non-destructive procedure, it does not alter the sample, making it suitable for sensitive materials, that includes shining a laser beam on a sample and measuring the amount of light reflected at various wavelengths. The principles of ORS are the light interaction, the spectral analysis and reflectance measurement. When light interacts with a material, various phenomena can take place, including reflection, absorption, and transmission. The degree of light that is reflected is influenced by the material's characteristics and the angle at which the light strikes the surface. The reflectance is defined as the ratio of the intensity of reflected light to the intensity of incident light (Figure 14). More specifically a light source (incident light) is directed onto the material at normal incidence. The reflection at the surface is characterised by the reflection coefficient, also known as reflectivity, typically represented by the symbol R. It is defined as the proportion of reflected intensity compared to the intensity of the source. The reflectance R is defined as:

$$R = \frac{I_R}{I_0} \quad (11)$$

where: I_0 is the incident light intensity and I_R is the reflected light intensity.

If there is no energy lost due to absorption or scattering, the conservation of energy dictates that the sum of reflectance and transmittance can approach unity.

$$R + T = 1 \quad (13)$$

The measurement is necessary to estimate the intensity I_0. To validate the measurement and estimate the intensity I_0, silicon is used as a reference material. The reflectance of silicon R_{Si} is calculated based on its intensity measurement:

$$R_{Si} = \frac{I_{Si}}{I_0} \quad (14)$$

The propagation of a beam through a transparent medium is governed by the refractive index, denoted as n. This is defined as the ratio of the speed of light in a vacuum (c) to its speed in the medium (v). The refractive index varies based on the frequency of the light beam. In colourless transparent materials such as glass, the dispersion is small in the visible spectral region, and it therefore makes sense to speak of 'the' refractive index of the substance in question.

Using reflectance properties and the relationship with the reference material, a simplified formula for the sample's reflectance is derived:

$$R = R_{Si} \frac{I_R}{I_{Si}} \quad (15)$$

ORS is commonly performed in the ultraviolet, visible, and near-infrared regions of the electromagnetic spectrum. Different materials have distinct reflectance characteristics in

this range, which can be applied for identification and characterisation. The reflectance of a material is affected by its complex refractive index, defined through the equation:

$$\tilde{n} = n + ik \quad (16)$$

where: n is the real part, representing the material's refractive property, and k is the imaginary part, representing the absorption coefficient. The reflectance at a given wavelength is determined by both n and k, and varies based on the wavelength of the incident light. This relationship enables ORS to offer spectral data that can be used to analyse material properties across a range of wavelengths. The reflectivity, which depends on both n and k, is expressed by the following equation (under normal incidence geometry):

$$R = \left|\frac{\tilde{n} - 1}{\tilde{n} + 1}\right|^2 = \frac{(n-1)^2 + k^2}{(n+1)^2 + k^2} \quad (17)$$

As regards to the mathematical models, Fresnel equations describe the reflectance and transmittance of light at an interface between two different media, depending on the angle of incidence and the refractive indices of the materials. [97] In a transparent material such as glass in the visible region of the spectrum, the absorption coefficient is very small. This is why tables of the properties of transparent optical materials generally list only the real parts of the refractive index and dielectric constant. If there is significant absorption, then the real and the imaginary parts are needed.[96]

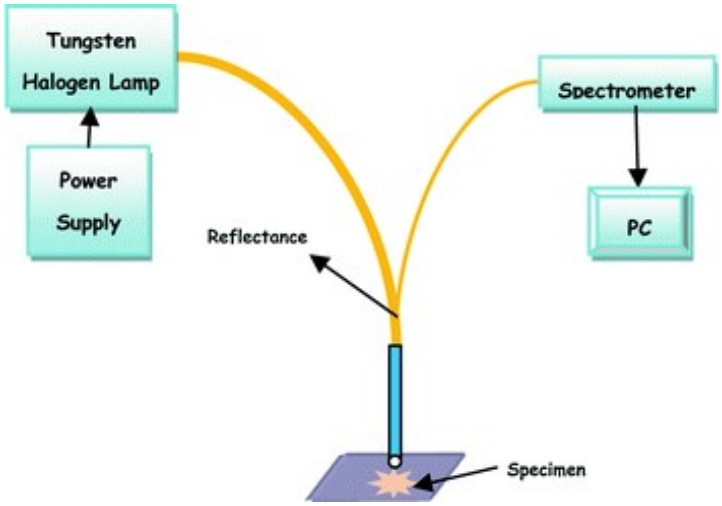


Figure 14. *Schematic of the set-up employed during an ORS measurement.*

The basic components of the ORS setup are the light source, the monochromator, the sample holder, the detector and the data acquisition system. The light source includes Tungsten-Halogen Lamps, Deuterium Lamps, LEDs or Lasers. It is essential the light source to emit a continuous spectrum to allow the spectral analysis. The monochromator is used to disperse the light into its component wavelengths. The sample must be securely

positioned at a consistent angle to the incident light. The detector captures the intensity of the reflected light. The data acquisition system collects the signals from the detector and converts them into digital data for analysis. The coordination and the control of the components are achieved through the computer. Optical Reflectance Spectroscopy is a versatile and valuable tool in both research and industrial applications. Its ability to provide detailed information about the optical properties of materials makes it essential in various scientific fields.

In this study, optical reflectance measurements were primarily conducted to determine SiO_2 film thickness. Optical properties of normal-incidence optical reflectance spectra were measured in the 250 – 900 nm. The lamp's spectral light intensity was recorded using a Si wafer as a reference sample. The spacing between the optical fibre head and the sample surface was adjusted to ensure maximum reflected intensity, and the number of counts was adjusted to keep the peak intensity below the detector's saturation limit. The light source was then closed to record the dark intensity. Subsequently, the source was reopened, the sample was placed under the probe, and the reflective light intensity of the measured sample, was recorded. Light is emitted from the source toward a point above the surface of a thin film material. The light is then reflected either from the surface of the thin film, the interface between the film and substrate, or after undergoing one or more internal reflections between the surface and the interface. A spectrometer detects reflected light based on photon energy. The occurrence of multiple internal reflections enables the film thickness to be determined by analysing the spacing of the interference fringes.[7] In this study, the thickness of the In_2O_3 film used in the TFT was systematically investigated to assess its impact on device performance. ORS was utilized as a reliable and accurate method for measuring the film thickness. By repeating the spin coating process under controlled conditions, films with one to five successive layers of the precursor solution were fabricated. This approach allowed for the precise control of film thickness, providing a clear understanding of the correlation between the number of deposited layers and the resulting thickness. Figure 15 illustrates this relationship, presenting a detailed plot of the measured thickness as a function of the number of spin-coated layers.

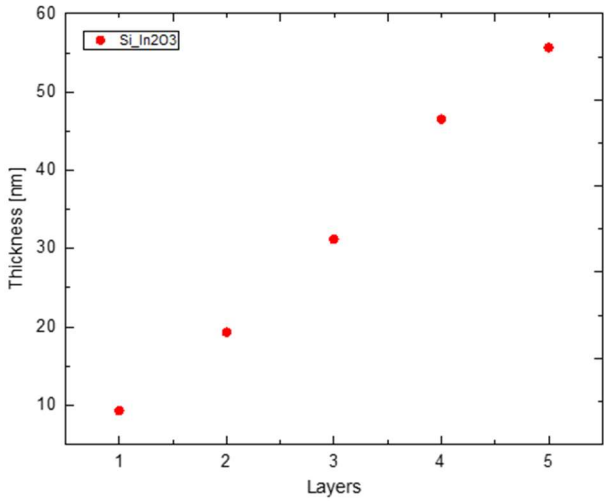


Figure 15. *Detailed plot of the measured thickness of the samples as a function of the number of spin-coated layers of In_2O_3 films.*

Below, in Figure 16 two representative reflectance curves along with their fittings are presented for a sample consisting of a single spin-coated layer. In the first case Figure 16(a), the deposited layer of In_2O_3 (10 nm) is on a Si substrate, while in the second Figure 16(b), it is a deposited layer of In_2O_3 (10 nm) on a commercial Si substrate with an additional coated layer of SiO_2. The fitting was performed using previously published data for the values of *n* and *k* of In_2O_3.

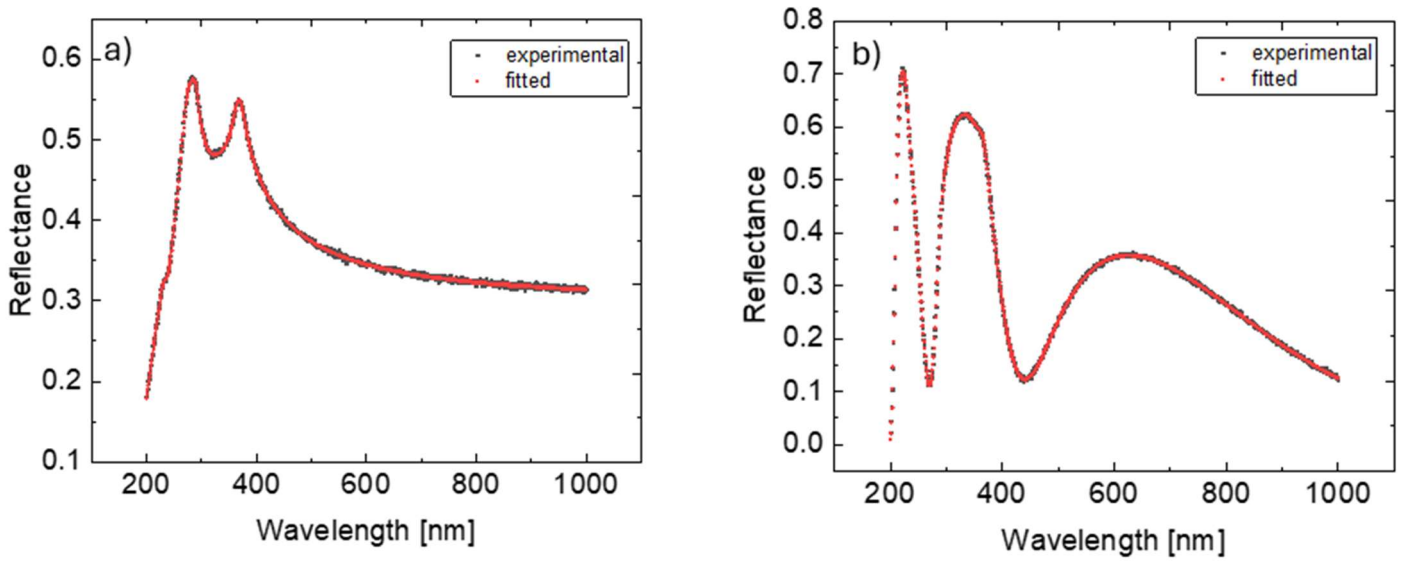


Figure 16. *Representative reflectance curves along with their fittings for a sample consisting of a single spin-coated layer of In_2O_3. a) Representative reflectance curve of a Si substrate with a deposited layer of In_2O_3 b) Representative reflectance curve of a commercial Si substrate with a thermal SiO_2 layer on top, additionally coated with a deposited In_2O_3 layer.*

Additionally, a measurement was carried out on a commercially available substrate featuring a SiO_2 film. The specified thickness of the SiO_2 layer is 200 nm. This measurement aimed to confirm the accuracy of the oxide layer's thickness, ensuring consistency with the reported value and validating the reliability of the measurement technique employed.

The Cauchy model is widely used in optical spectroscopy to describe the wavelength dependence of the refractive index of transparent materials. It is particularly useful for characterising thin films in optical reflectance spectroscopy. The refractive index $n(\lambda)$ as a function of wavelength λ is expressed by the Cauchy equation:

$$n(\lambda) = A + \frac{B}{\lambda^2} + \frac{C}{\lambda^4} + \cdots \qquad (18)$$

where A, B, and C are material-dependent coefficients determined experimentally. The parameter A represents the refractive index at long wavelengths, while B and C account for the dispersion of the material. but they have different contributions. B is the dominant dispersion coefficient in the visible and near-infrared regions, while C refines the dispersion

behaviour further, especially as wavelengths approach the ultraviolet range. The reflectivity plots were generated using the Cauchy model. The material-dependent coefficients were considered as follows: A=1.452 and B=0.00391, while the coefficient C was not fitted, as it did not contribute significantly to the accuracy of the model. Figure 17(a) presents the plot of reflectivity of a commercially available substrate featuring a SiO_2 film. Figure 17(b) represents the refractive index as a function of the wavelength of this sample. Following this investigation, the use of a single deposited layer was selected for the device fabrication.

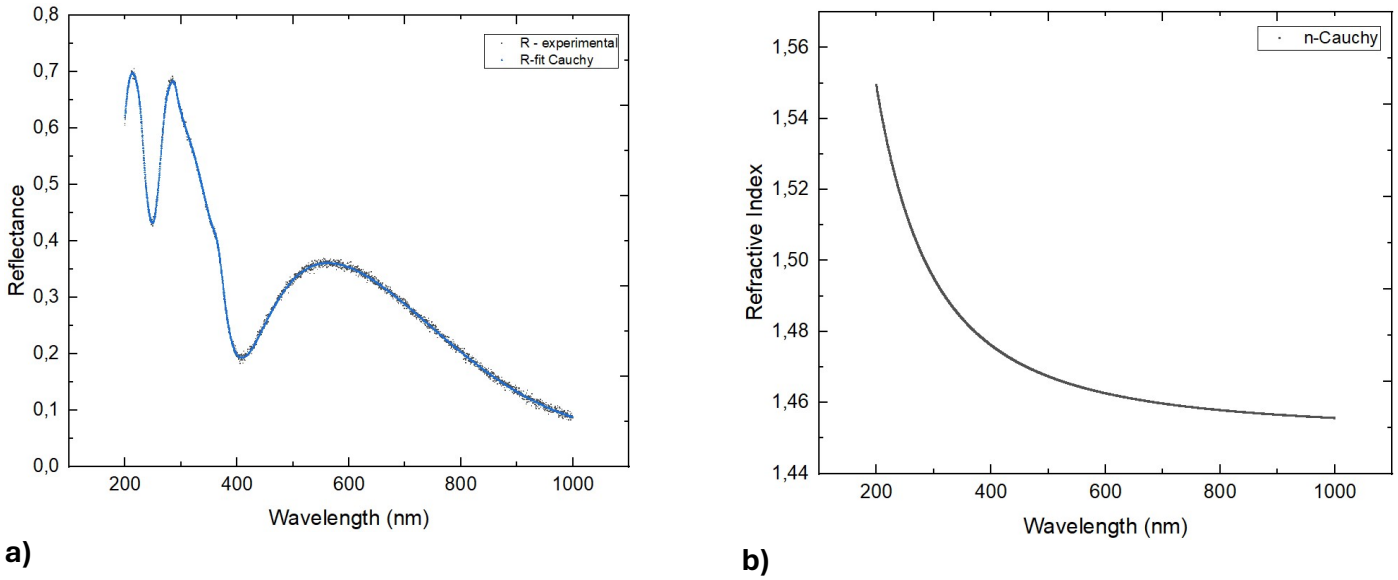


Figure 17. Plots of the reflectivity a) The figure presents the plot of reflectivity of a commercially available substrate featuring a SiO_2 film. The Cauchy model was used for the fitting. b) Plot of the refractive index as a function of the wavelength of a commercially available substrate featuring a SiO_2 film.

5. Electrical Characterisation and Statistics of the devices

Two representative sets of transfer and output characteristics are presented below, with additional measurements available in the Appendix. Notable differences between these two samples emphasize the importance of the following statistical analysis in assessing the effectiveness of the transistor fabrication method. Figure 18(a) presents the transfer characteristics of two of the TFT devices that were fabricated for this work. The transfer curves are showing drain current as a function of gate bias. The gate-source voltage, V_{GS}, ranges from -60V to 60V and back to -60V. As shown in Figure 18 (a) the devices exhibit a small hysteresis in the transfer curves. This is seen as the forward (increasing V_{GS}) and reverse (decreasing V_{GS}) sweeps are not overlapping. Hysteresis is represented by the difference between these sweeps, especially in the region where the current I_{DS} is rising significantly. This hysteresis is indicative of charge trapping effects within the device, leading to a shift in threshold voltage between the forward and reverse sweeps. More specifically, hysteresis in oxide-semiconductor TFTs is often attributed to charge trapping in the gate dielectric (SiO_2) or at the semiconductor/dielectric interface. This trapped charge can shift

the apparent threshold voltage, creating hysteresis as the traps fill and empty during the voltage sweeps. The negligible hysteresis observed in all curves cannot be attributed to carrier trap sites caused by incomplete conversion of the precursor into pure metal oxide. This is because full conversion is achieved through thermal annealing at 300°C for one hour.

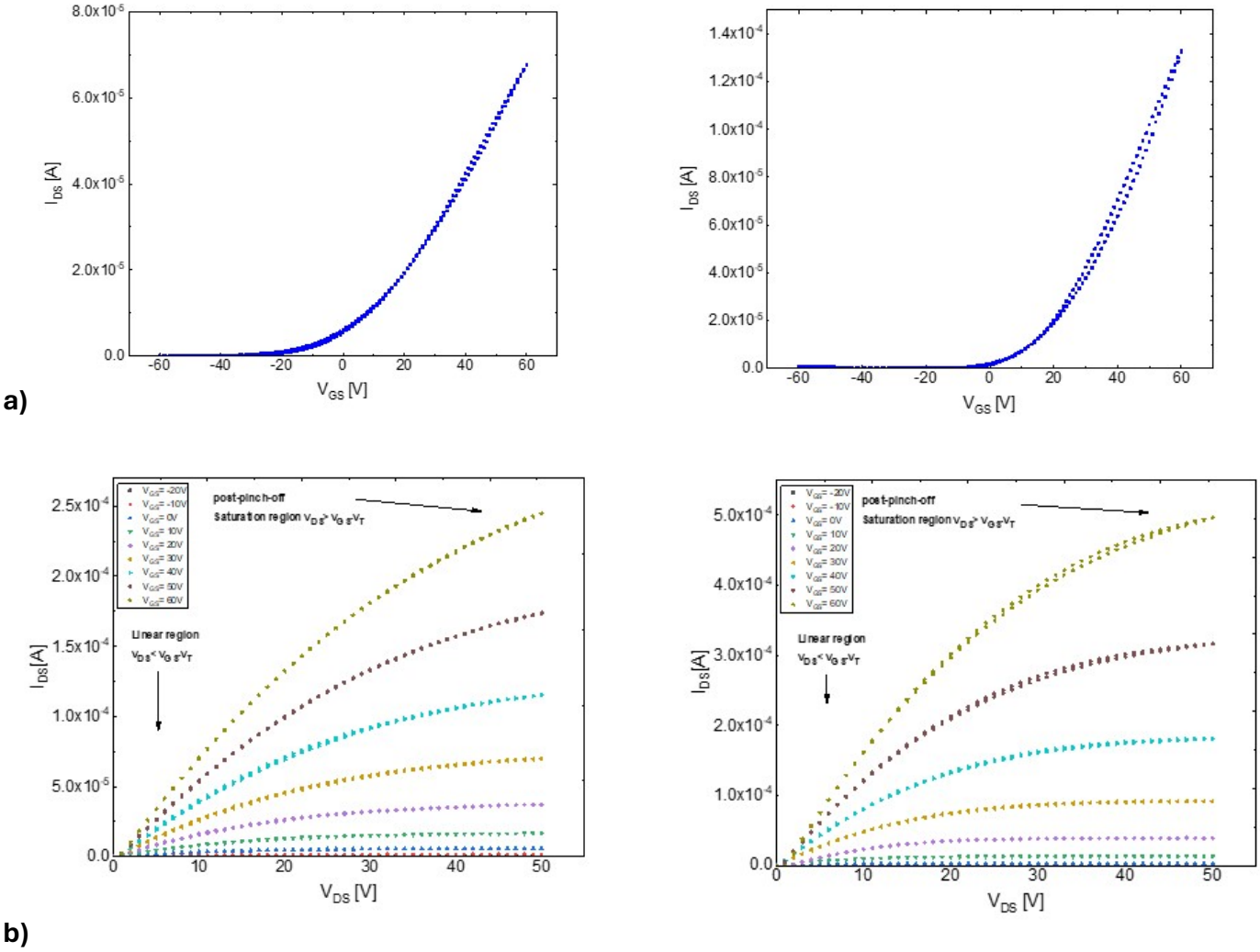


Figure 18. *a) Transfer (blue) characteristic of BGTC TFT devices (TFT 9 and TFT 10) based on thermally annealed (300 °C, 60 min) sol-gel In_2O_3 thin films on commercial Si substrates with a SiO_2 layer. Drain voltage (V_{DS}) was maintained at 5V during transfer measurements, to account for linear region operation The gate voltage (V_{GS}) ranges from -60V to 60V and back to -60V during the forward and reverse voltage sweep. b) The different curves, distinguished by colour, represent the output characteristics (TFT 9 and TFT 10) for varying input conditions, with each colour corresponding to a different input voltage as indicated in the legend. Gate voltage (V_{GS}) ranged at $-20 \leq V_{GS} \leq 60$ V over output measurements, with a step of 10 V.*

Figure 18(b) displays the output characteristics of the devices. The output curves are showing the linear and saturation operating regimes, as expected for a TFT. The gate voltage range was restricted to $-20 < V_{GS} < 60$ V, in steps of 10V. A clear transition from the linear to the saturation region is noticed in all TFTs (above threshold voltage). I_{DS} values typically range from the low 10^{-5} A to the mid 10^{-4} A. The maximum I_{DS} can be influenced by various factors,

including the quality of spin-coating and environmental conditions like temperature and humidity, with the $InNO_3$ precursor being particularly sensitive to these variations. Increasing the gate voltage (V_{GS}) shifts the saturation current upwards, which reflects good modulation of the channel by the gate voltage. The different curves represent various V_{GS} values (from -20 V to 60 V), and it is shown that as V_{GS} increases, the saturation current I_{DS} also increases. This is expected, as a higher V_{GS} strengthens the channel, allowing more current to flow. This strong gate control over the channel current is a positive indicator of the transistor's effectiveness in modulating conductivity. There are some small irregularities in the curves, which might indicate minor issues such as contact resistance, trapping effects, or inconsistencies in the In_2O_3 film. These irregularities are represented by hysteresis, which is illustrated by the difference between the sweeps, especially in the region where the current I_{DS} increases significantly. Figure 18(b) shows that for small values of V_{DS}, channel current (I_{DS}) flows through the device. As we increase V_{DS}, I_{DS} will increase until the device channel current reaches saturation. Under these operating conditions, where the applied V_{DS} is significantly smaller than V_{GS}, we see the linear I–V relationship, and the device is said to be operating in the linear regime. When the electric field strength parallel to the device channel V_{DS} is comparable to that created by the gate voltage V_{GS}, the field across the dielectric is too weak to sustain charge accumulation near the drain end of the device. As a result, the region near the drain contact loses charge carriers, leading to what is known as "pinch-off" in the channel. Under this condition, I_{DS} becomes V_{DS} independent, and the device operates through a saturation regime(Figure 3) .[18]

Transfer characteristics of the devices obtained by plotting the measured $(I_{DS})^{1/2}$ as a function of applied V_{GS}, at a constant V_{DS} (Figure 19). These plots were utilized to determine the threshold voltage. Details of the linear fit of these two samples are presented in Table 1. Measurements can be performed at any two distinct V_{DS} values that capture both the linear and saturation regimes, resulting in two different maximum I_{DS} values. The drain voltage (V_{DS}) was maintained at 10V during the transfer measurements to ensure operation within the linear region. This value was selected based on observations of the output curves and have proven to be effective and reliable. [19, 20] In Figure 19 the linear fits (in red) in the active regions align well with the measured data, showing good consistency in the linear region. This suggests that the devices have stable and predictable transfer characteristics. All these variations observed in the transfer and output characteristics of transistors fabricated under the same conditions make the statistical analysis presented later in this chapter particularly interesting.

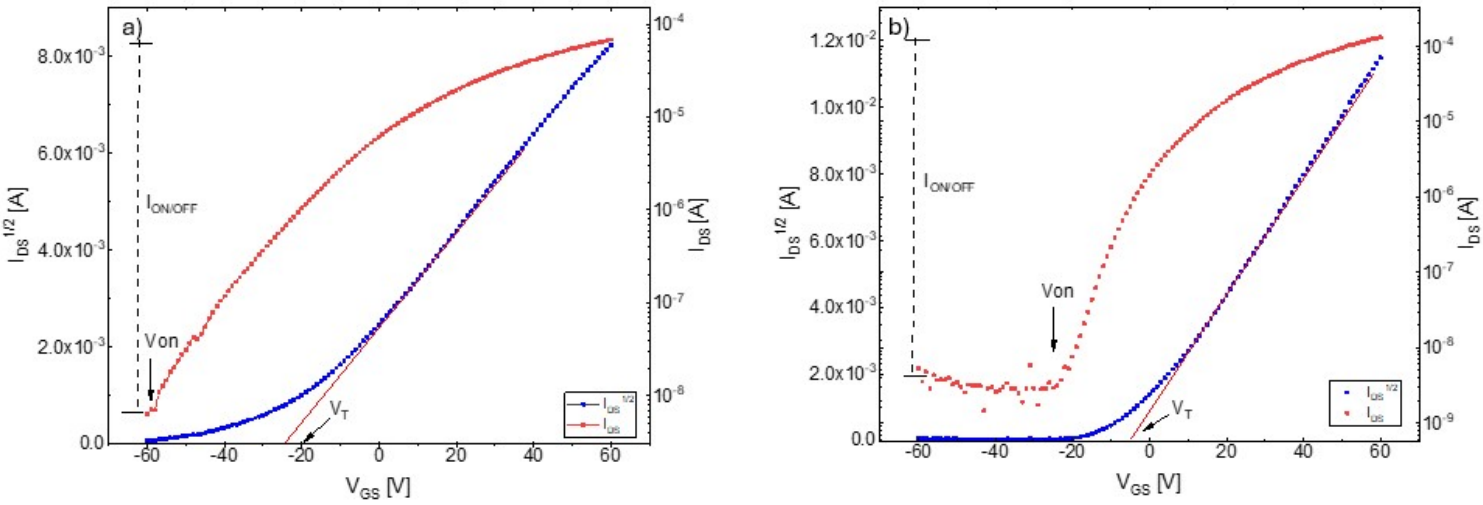


Figure 19. *Transfer characteristics of two different transistors a) TFT 9 b) TFT 10 that were fabricated under the same conditions in this work, showing the square root of the drain current ($I_{DS}^{1/2}$, left y-axis) (blue) and the absolute drain current (I_{DS} right y-axis) in logarithmic scale (red) as a function of the gate-source voltage (V_{GS}). The gate voltage (V_{GS}) is swept from -60V to 60V. The threshold voltage (V_T) obtained through a linear fit (red straight line) to the $I_{DS}^{1/2}$ curve, as indicated in the plot. The turn-on voltage (Von) and the ON/OFF current ratio ($I_{ON/IOFFI}$) are also marked.*

Equation	y=a +b*x	Equation	y=a +b*x
Plot	$I_{DS}^{1/2}$ - V_{DS} (TFT 9)	Plot	$I_{DS}^{1/2}$ - V_{DS} (TFT 10)
Intercept	0,00249	Intercept	7,90529E-4
Slope	9,68781E-5	Slope	1,79136E-4
Residual Sum of Squares	3,29408E-8	Residual Sum of Squares	1,80207E-8
Pearson's r	0,99974	Pearson's r	0,99995
R-Square (COD)	0,99947	R-Square (COD)	0,9999
Adj. R-Square	0,99946	Adj. R-Square	0,9999

Table 1. *Details of the linear fit (red straight line) of the plots in Figure 19(a) and Figure 19(b) that were used to determinate the threshold voltage (V_T) of the transistors.*

The most important parameters of the TFT device can be extracted from the output and transfer curves. These parameters include the threshold voltage (V_T), on/off current ratio ($I_{on/off}$), subthreshold swing (SS), turn-on voltage (V_{ON}), and charge carrier mobility (μ). By using the experimentally obtained data one can extract all the necessary parameters. In this work, the values of threshold voltage (V_T), charge carrier mobility (μ) and on/off current ratio ($I_{on/off}$) and the subthreshold swing are calculated for the electrical characterisation of the devices. The threshold voltage (V_T) is the voltage at which a thin-film transistor starts forming a conductive channel between the source and drain electrodes. This V_T corresponds to the gate-source voltage V_{GS} at which a carrier channel is established within the semiconductor near the oxide-semiconductor interface. V_T is typically determined through linear

extrapolation of the I_{DS}–V_{GS} transfer curve at low V_{DS} values or from the $I_{DS}^{1/2}$–V_{GS} plot at higher V_{DS} values. [2122] The threshold voltage varies from -36.3 V to 4.33 V across the samples. Table 2 shows the calculated values of the threshold voltage, the on/off ratio and the mobility of the transistors and Table 3 shows the mean, the range and the standard deviation for the values of the threshold voltage, the linear mobility and the on/off ratio.

TFTs	Threshold Voltage [V]	Linear Mobility [cm^2/Vs]	On/Off Ratio	Subthreshold Swing
TFT 1	4.33	4.66	3061120	0.084
TFT 2	-2.92	3.68	81	0.89
TFT 3	-4.8	9.1	61	0.94
TFT 4	-3.76	4.11	98	0.74
TFT 5	0.43	3.42	138	0.71
TFT 6	-16.38	1.44	17	1
TFT 7	-4.25	2.93	54	1
TFT 8	-10	1.8	200	0.87
TFT 9	-25.7	1.55	9729	1
TFT 10	-4.4	3.5	47694	0.23
TFT 11	-18.1	1.12	292984	0.14
TFT 12	-6.8	1.17	168	1
TFT 13	-26.2	1.52	8169	0.6
TFT 14	-36.3	2.74	195	1
TFT 15	-32	0.93	28	1
TFT 16	-10	2.4	23	0.9

Table 2. *Calculated values of the threshold voltage, the on/off ratio, the mobility and the subthreshold swing of the transistors that were fabricated in this work.*

	Mean	Range	Standard Deviation	Median
Threshold Voltage	-12.3	40.63	12.14	-8.4
Linear Mobility	2.87	8.17	2.03	2.57
On/Off Ratio	263130	3061066	844523	195
Subthreshold Swing	0	0.91	0.31	0.88

Table 3. *Values of the mean, the range, the standard deviation and the median for the calculated values of the threshold voltage, the linear mobility, the on/off ratio and the subthreshold swing of the transistors that were fabricated in this work.*

Threshold voltage (V_T)

Sample TFT 14 has the lowest V_T at -36.3 V, suggesting it requires the least gate voltage to turn on. Table 3 shows that the mean threshold voltage is -12.3, while the median is -8.4. The median value, being closer to zero than the mean, suggests a skew in the data towards more negative threshold voltages. These values are close, suggesting a relatively symmetric

distribution of threshold voltages among your transistors. With a standard deviation of 12.14 and a range of 40.63, there is some variability in the threshold voltage across the samples, but it remains within a manageable spread. The standard deviation relative to the mean highlights considerable variability, indicating that some devices deviate significantly from the central value.

On/Off Ratio ($I_{on/off}$)

The on-current (I_{on}) is the drain current (I_{DS}) that flows through a thin-film transistor when it is in the "on" state. Higher I_{on} values are desirable, as they enhance switching speeds and improve TFT performance by enabling strong load-driving capability. Conversely, the off-current (I_{off}) is the leakage current present when the TFT is switched "off." Lower I_{off} values are beneficial for reducing power consumption and improving efficiency. The $I_{on/off}$ ratio is defined as the ratio of I_{DS} in the on-state to that in the off-state. A high on/off current ratio is crucial, as it indicates the TFT's ability to effectively control I_{DS} and efficiently switch between states. This high ratio benefits both analog and digital circuit designs by reducing leakage currents, minimizing channel crosstalk, lowering static power consumption, enhancing driving capabilities, and increasing switching speeds.[22] The on/off current ratio ($I_{on/off}$) can be directly obtained from transfer curves (logarithmic scale). This is a unitless measure of the ratio of two channel current values, typically between the noise floor level and fully-on at a specified V_{GS}. Here, the minimum I_{DS} typically corresponds to the measurement's noise level, while the maximum I_{DS} depends on the semiconductor's properties.[21] As regards the on/off ratio values, TFT 1 has excellent switching behaviour while sample TFT 6 shows a really low on off ratio. This shows that the device may have issues such as leakage current, which allows some current to flow even in the "off" state. Figure 19 shows, for the two samples, the logarithmic scale for I_{DS}, which is valuable for analysing both the on-state and off-state currents and determining the on/off ratio. A high on/off ratio indicates strong gate modulation and is essential for switching applications where clear distinctions between the on and off states are required. There's a slight fluctuation in the I_{DS} values in the off state, which could be due to measurement noise or small leakage paths within the devices. These fluctuations are minor, though, and do not significantly impact on the overall performance, as the off-state current remains very low. As regards the on/off ratio values, Table 2 shows that the mean of on/off ration and the median are close. The standard deviation is very high, indicating substantial variability in the on/off ratio across the samples. The high variability in the on/off ratio might point to inconsistencies in fabrication that affect how well each transistor can switch off.

Mobility (μ)

The charge carrier mobility is arguably the most significant metric by which different semiconductor technologies and the resulting TFT devices are assessed. Mobility is crucial in TFTs because higher mobility enables a larger source-drain current (I_{DS}) over a specified range of gate voltage (V_{GS}) for a given source-drain voltage (V_{DS}). Linear and saturation mobilities can be determined from the transfer curve, with mobility ideally measured from a transfer curve that shows linearity across a broad gate voltage range. In the linear regime, the I_{DS}–V_{GS} relationship should be linear, as should $I_{DS}^{1/2}$–V_{GS} in the saturation regime. If linearity

is not achieved, special correction methods may be required to avoid overestimating mobility. Given that determining V_T can sometimes be uncertain, V_{ON} can be used as an alternative parameter to describe the gate voltage required to turn the device on. V_{ON} represents the point at which I_{DS} begins to flow due to charge accumulation induced by the electric field at the semiconductor/dielectric interface. High mobility often translates to faster device performance, which is crucial in applications like displays and sensors. [23] [21] As previously mentioned regarding the samples whose characteristics were presented in Figure 4, additional data on mobility and subthreshold swing are provided here. To calculate the mobility in the linear regime, the corresponding equation was employed (Equation 1). A plot of I_{DS} as a function of $((V_{GS}-V_T)\ V_{DS})$ - $V_{DS}^2/2$ was generated, as shown in Figure 20(b). The details of the linear fit for this plot are provided in Table 4. The slope of the linear fit was determined, and this slope is related to the mobility μ by the following Equation 18:

$$slope = \frac{\mu\, W\, \varepsilon_0\, \varepsilon_r}{2\, L\, t_{ox}} \quad (18)$$

where W is the channel width, L is the channel length, ε_0 is the permittivity of free space, ε_r is the relative permittivity of the gate dielectric, and t_{ox} is the thickness of the gate dielectric. Using this relationship, the mobility in the linear regime was extracted.

The analysis of the TFT mobility data reveals a mean value of 2.87. This is very close to the median of 2.57, suggesting a reasonably symmetric distribution of mobility values. The standard deviation (2.03) and the range of 8.17 between the highest and lowest mobility values indicate a moderate level of variability in mobility. The variance (2889.82) suggests some diversity in mobility values. Mobility values vary more than threshold voltage but remain within a reasonable range. In the related literature, it is observed that for In_2O_3 TFTs fabricated using the sol-gel method with indium nitrate, the typical linear mobility ranges from 1 $cm^2/V{\cdot}s$ to 10 $cm^2/V{\cdot}s$, with some optimized films reaching up to 20 $cm^2/V{\cdot}s$. These values are generally lower compared to those of TFTs fabricated using techniques such as sputtering.[24, 25]

In this work only the linear mobility is calculated, the mobility values in the saturation region are significantly lower. In the linear region, charge carriers (electrons or holes, depending on the TFT type) move freely through the channel, resulting in low resistance. As a result, mobility is higher in this region compared to the saturation region. In the saturation region, the electric field across the channel becomes strong enough to cause the channel to "pinch off" or restrict, reducing the carrier flow. Here, the carriers travel under a stronger electric field, leading to increased collisions, which ultimately reduces their mobility. Pinch-off occurs because an increase in V_{DS} reduces the number of carriers able to pass through the channel, as the channel near the source narrows. This results in fewer collisions between the carriers and the material's atoms, further decreasing mobility.[26, 17]

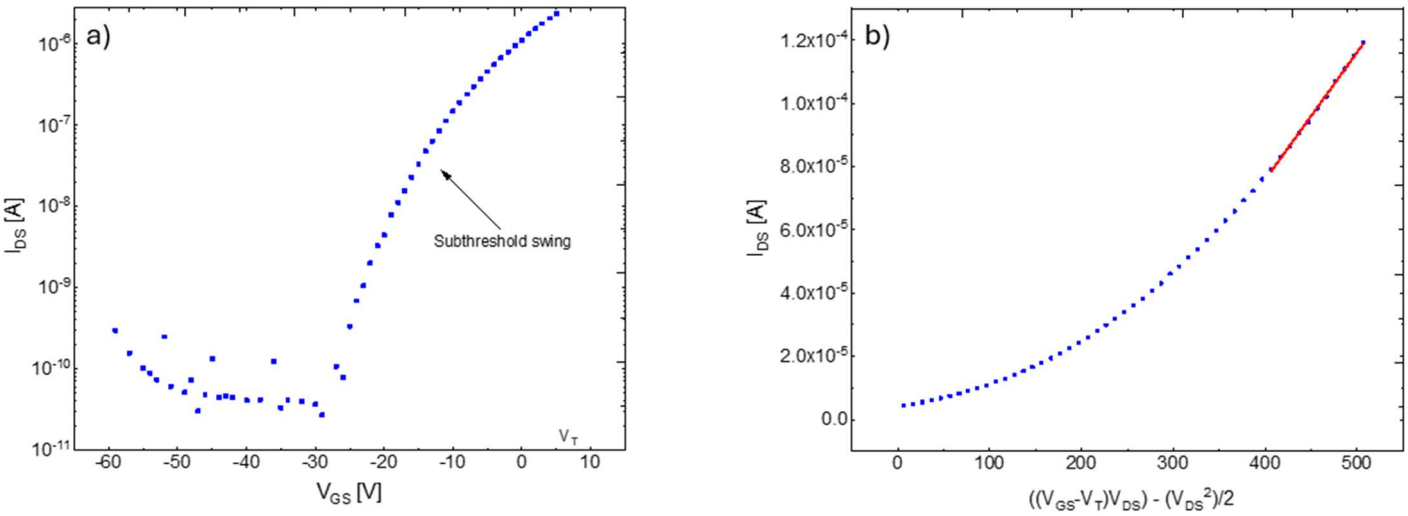


Figure 20. *a) Transfer characteristic of a transistor (TFT 1), showing the drain current (I_{DS}) as a function of the gate voltage (V_{GS}) on a logarithmic scale, for voltage values below the threshold voltage (V_T). The plot highlights the subthreshold region, with the subthreshold swing indicated. b) The plot represents the drain current (I_{DS}) as a function of ($(V_{GS}-V_T)\ V_{DS}$) - $V_{DS}^2/2$. The slope of the curve, obtained through a linear fit (red line), is crucial for calculating the mobility of the transistor.*

Equation	y=a +b*x
Plot	I_{DS} - ((V_{GS}-V_T) V_{DS}) - (V_{DS}^2)/2
Intercept	-8.5062E-5
Slope	4.02405E-7
Residual Sum of Squares	2.0987E-12
Pearson's r	0.99941
R-Square (COD)	0.99882
Adj. R-Square	0.99869

Table 4. *Details of the linear fit of the plot in Figure 20(b)*

Subthreshold Swing

The subthreshold regime is defined by the inverse slope S of the logarithmic I_{DS} - linear V_{GS} plot, measured in volts per decade. This represents the voltage needed to alter the current by one order of magnitude. This method is commonly employed in TFT characterisation, where, for a given gate capacitance, a smaller S indicates a higher-quality device. The subthreshold region provides insight into how steeply the current decreases with changes in gate bias.[27] The units of the subthreshold swing are typically expressed in volts per decade (V/decade). The operating voltage of thin-film transistors is closely linked to the subthreshold swing, a critical performance parameter that indicates the change in gate voltage (V_{GS})

required to achieve a tenfold increase in the drain current (I_{DS}). Subthreshold swing reflects the device's sensitivity to V_{GS} variations and its ability to switch on and off efficiently, particularly in low-power applications. A smaller subthreshold swing is highly desirable, as it enables TFTs to operate at lower voltages, enhances switching efficiency, and reduces power consumption. This is because a lower subthreshold swing allows the device to transition between on and off states with a smaller voltage swing, facilitating faster switching speeds.[15] To achieve a reduced subthreshold swing and lower operating voltages, the development of TFTs with high-capacitance gate dielectrics has emerged as a key focus for researchers in both industry and academia.[28] The subthreshold swing is calculated using the derivative method by analysing the transfer characteristics of the thin-film transistor. First, the logarithm of the drain current I_{DS} is plotted against the gate voltage V_{GS} to identify the subthreshold region, where the current increases exponentially with gate voltage. The first derivative is calculated in this region to determine the slope. The subthreshold swing is then obtained as the inverse of the maximum slope. Figure 20(a) shows the logarithmic scale of I_{DS} as a function of the V_{GS}. In this plot it is shown the subthreshold swing. The mean value is 0, indicating that, on average, the subthreshold swing values across the transistors are very close to zero. This suggests an excellent switching performance for some devices, as an SS approaching zero is desirable in TFTs for low-power and efficient operation. The range of 0.91 highlights a significant spread between the lowest and highest subthreshold swing values. The standard deviation of 0.31 indicates a moderate dispersion of subthreshold swing values around the mean. This level of variability suggests that while some devices are performing well, there is noticeable inconsistency across the dataset. The subthreshold swing in sol-gel thin-film transistors can often exceed 1 V/decade due to material properties and fabrication-related issues. Several factors contribute to this behaviour, preventing the device from achieving ideal performance. The sol-gel process may introduce defects or trap states in the semiconductor or at the interface with the gate dielectric, which adversely affect electrical performance. Additionally, sol-gel films often exhibit grain boundaries or other imperfections that degrade their quality. Environmental factors, such as humidity and contamination during fabrication, can further impact the sol-gel film, introducing additional trap states. Defects may also arise during the spin coating process, and imperfections in the substrate itself can further exacerbate these issues. Together, these factors contribute to the larger subthreshold swing values observed in some sol-gel TFTs.

	Threshold Voltage	Linear Mobility	On/Off Ratio	Subthreshold Swing
Threshold Voltage	1	0.5	0.3	0.4
Linear Mobility	0.5	1	0.2	-0.003
On/Off Ratio	0.3	0.2	1	-0.5
Subthreshold Swing	0.4	-0.003	-0.5	1

***Table 5. Correlation** matrix **of the calculated values** displaying the relationships between the variables. The colour intensity indicates the strength of the correlation, with green representing stronger correlations.*

Table 5 shows the correlation matrix of the calculated values. This correlation matrix provides valuable insights into the relationships between the parameters for the transistors. The correlation coefficients were calculated. Values close to 1, shows a strong positive correlation, while values close to -1, shows a strong negative correlation. The weak negative correlation suggests a very slight inverse relationship between the subthreshold swing and the on/off ratio. This indicates that these two metrics are largely independent. The strongest relationship here is the positive correlation between threshold voltage and linear mobility. This can be also verified by the equation that gives us the mobility in the linear region. A positive correlation between the subthreshold swing and the threshold voltage. This can be also verified by the methodology that is used to calculate the subthreshold swing values. It is shown also a strong negative correlation between the on/off ratio and the subthreshold swing. Moreover, the correlation matrix shows a weak positive correlation between the linear mobility and the on/off current ratio.

6. Conclusions and Future Perspectives

Conclusions

The extracted mobility values from the fabricated transistors were compared with those reported in the literature for devices using the same material but fabricated with different methods. The measured mobilities exhibit a range from 0.93 to 9.1 cm^2/Vs, with an average value of 2.88 cm^2/Vs, while literature reports mobility values between 1 and 24 cm^2/Vs, depending on the fabrication technique. TFTs using high-temperature thermal annealing or a combination of thermal and optical annealing have been reported in recent years. Indium oxide transistors made via single-step laser-induced photochemical conversion of a sol-gel precursor achieve mobilities up to 13 cm^2/Vs.[19] The observed differences highlight the influence of the deposition method, processing conditions, and interface quality on charge transport properties. While direct comparison is challenging due to variations in fabrication techniques, the results provide valuable insight into how different processing approaches affect device performance. Further optimization of the fabrication process could help improve mobility and align it more closely with the highest reported values for this material. The sol-gel process can introduce defects or trap states in the semiconductor or at the gate dielectric interface, negatively impacting electrical performance. Additionally, sol-gel films often contain grain boundaries and other imperfections that degrade their quality. Environmental factors, such as humidity and contamination during fabrication, can further deteriorate the film by introducing additional trap states. Moreover, defects may form during spin coating, while substrate imperfections can further exacerbate these issues.

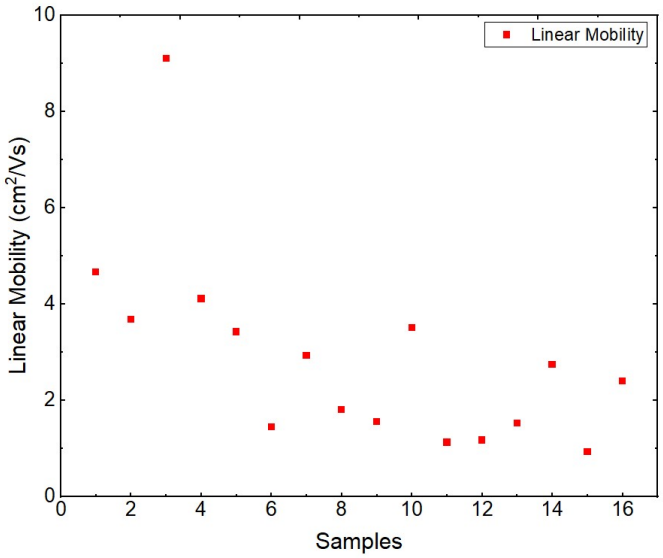


Figure 21. *Mobility spread plot of the transistors fabricated in this work, showing a maximum value of 9.1 $cm^2/V{\cdot}s$ and a minimum value of 0.93 $cm^2/V{\cdot}s$.*

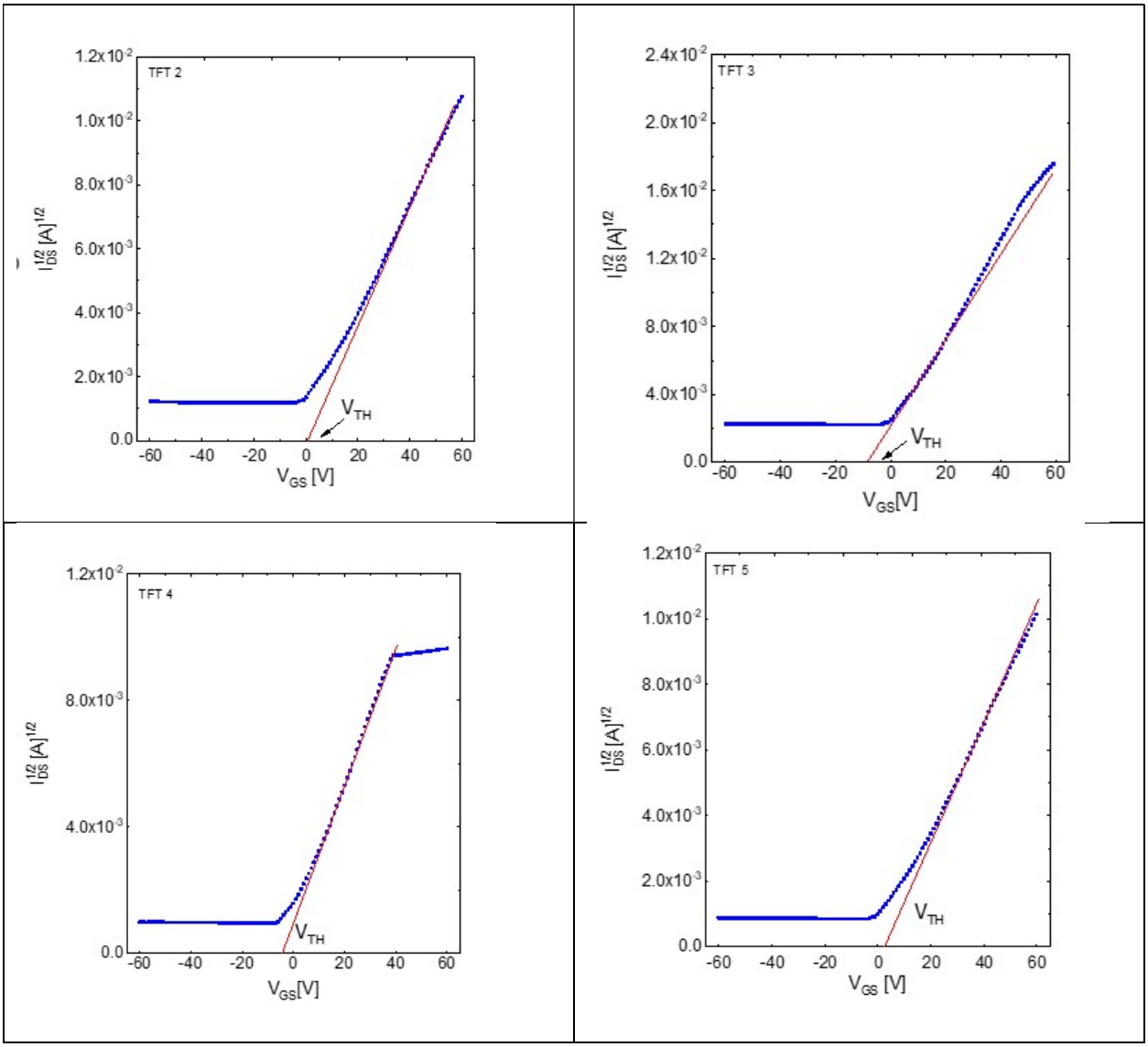
The mobility spread plot in Figure 21 illustrates the variation in linear mobility across different samples. A significant dispersion in mobility values is observed. Some samples exhibit notably high mobility, while others show lower values, suggesting the presence of inconsistencies in material quality or interface properties. Since all transistors were fabricated under the same conditions, the observed mobility variations suggest that other factors, such as intrinsic material properties, local defects, interface states, or slight process fluctuations, may influence the device performance. The spread in mobility values indicates that even under controlled fabrication, inherent variations can arise, potentially due to differences in film morphology, grain boundaries, or charge trapping effects. These findings highlight the importance of further refining processing techniques and characterising material properties to achieve more consistent and reproducible transistor performance.

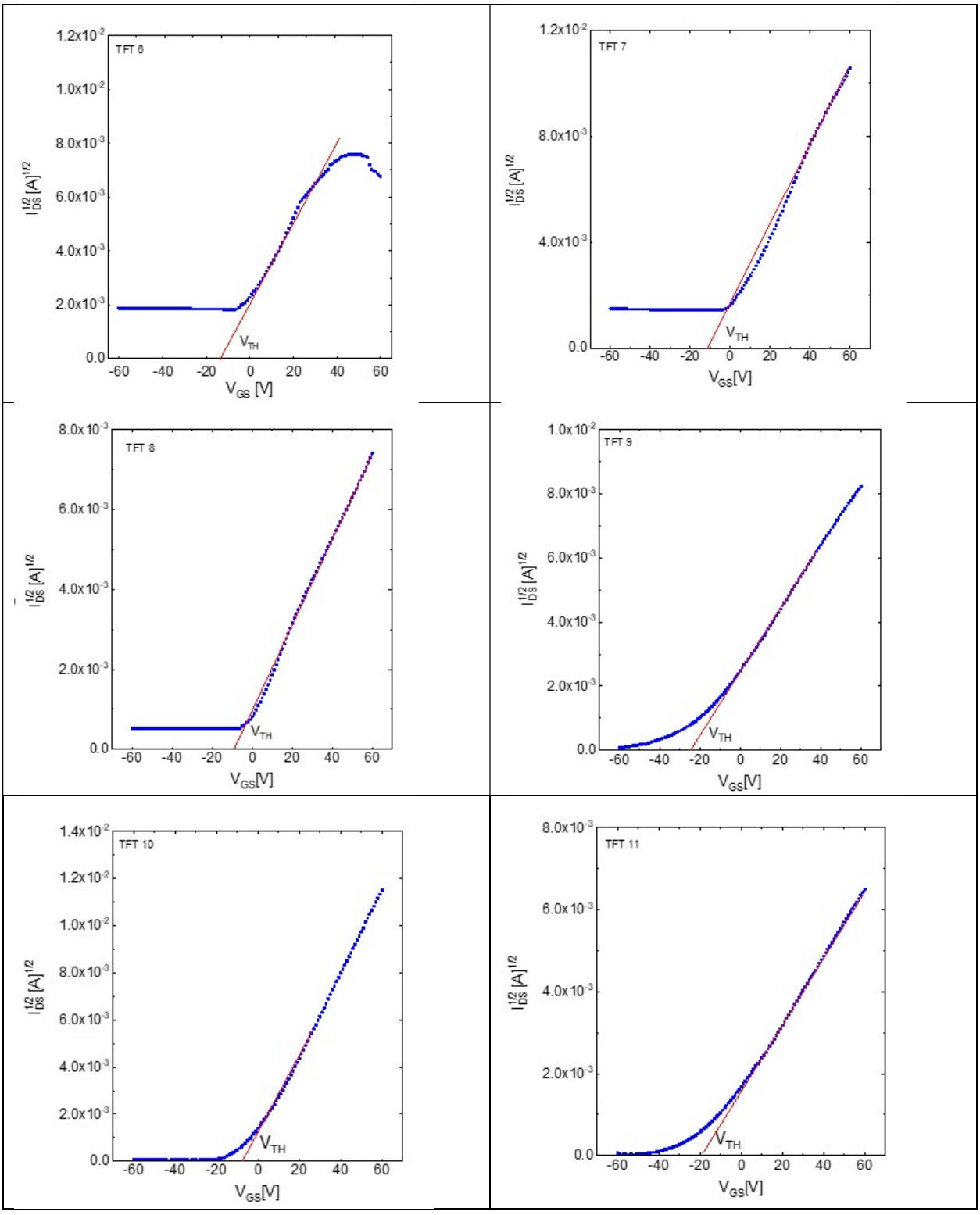
Future Perspectives

- A future objective is to implement rapid thermal annealing in a controlled atmosphere to achieve better process control, minimize by-product formation, and improve hysteresis. Additionally, low V_{GS} voltages are desirable, as higher V_{GS} levels lead to increased power consumption.
- Replacing 2-ME with water for environmentally friendly fabrication reduces solvent waste but requires re-optimizing LA conditions.
- Printing-based deposition methods, such as inkjet printing, slot-die, and spray coating, can replace spin coating for dielectric and semiconductor films. Combined with LA, this approach enables high-performance electronics while ensuring compatibility with large-scale fabrication.

Appendix: Additional Plots

This appendix presents additional plots that support the data analysis in Chapter 5.

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TFT 9
TFT 10
TFT 11
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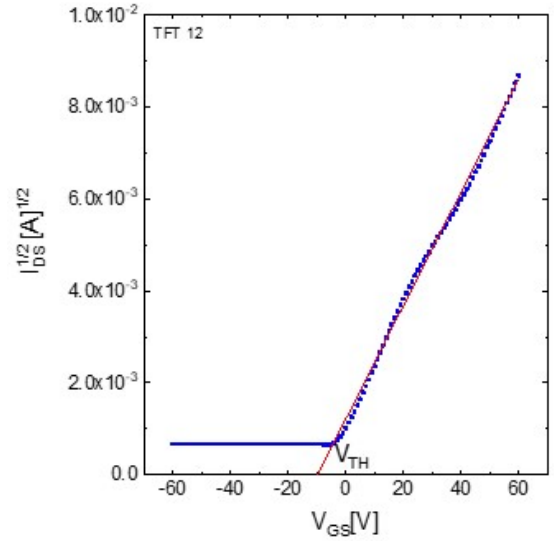
V_{GS} [V]
V_{TH}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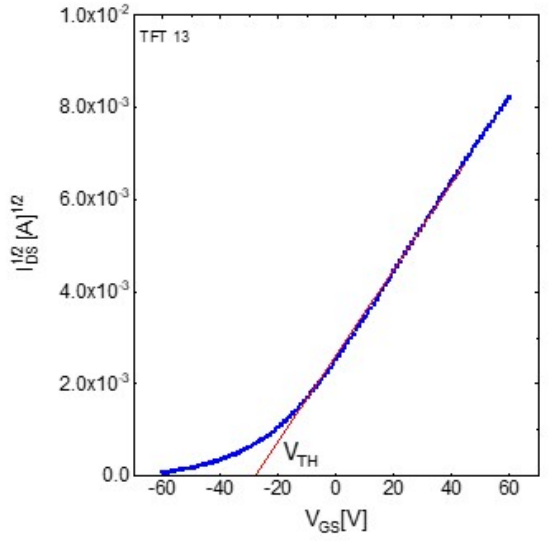
$I_{DS}^{1/2}$ [A]$^{1/2}$
V_{GS}[V]
V_{TH}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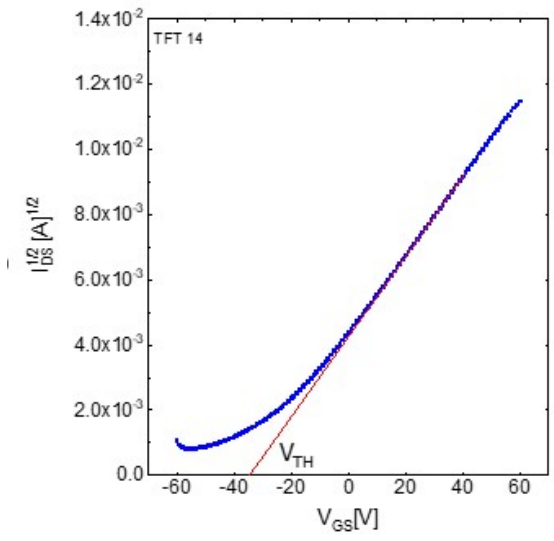
$I_{DS}^{1/2}$ [A]$^{1/2}$
V_{GS}[V]
V_{TH}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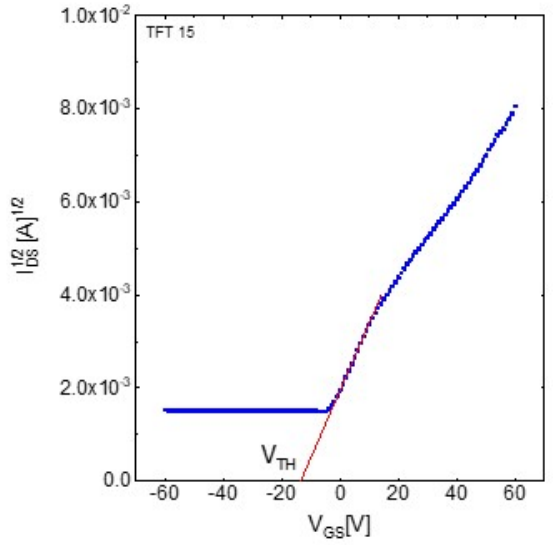
$I_{DS}^{1/2}$ [A]$^{1/2}$
V_{GS}[V]
V_{TH}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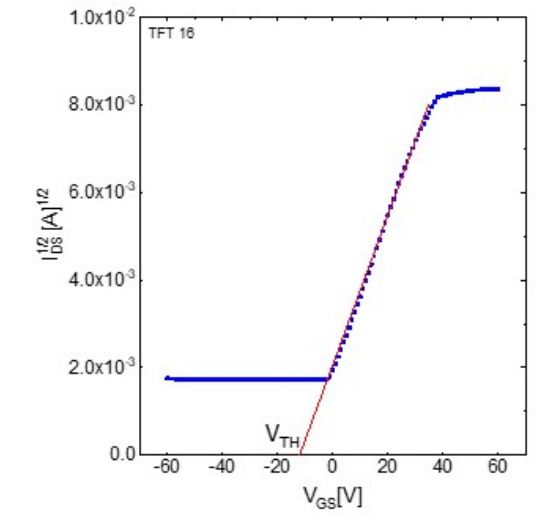
V_{GS}[V]
V_{TH}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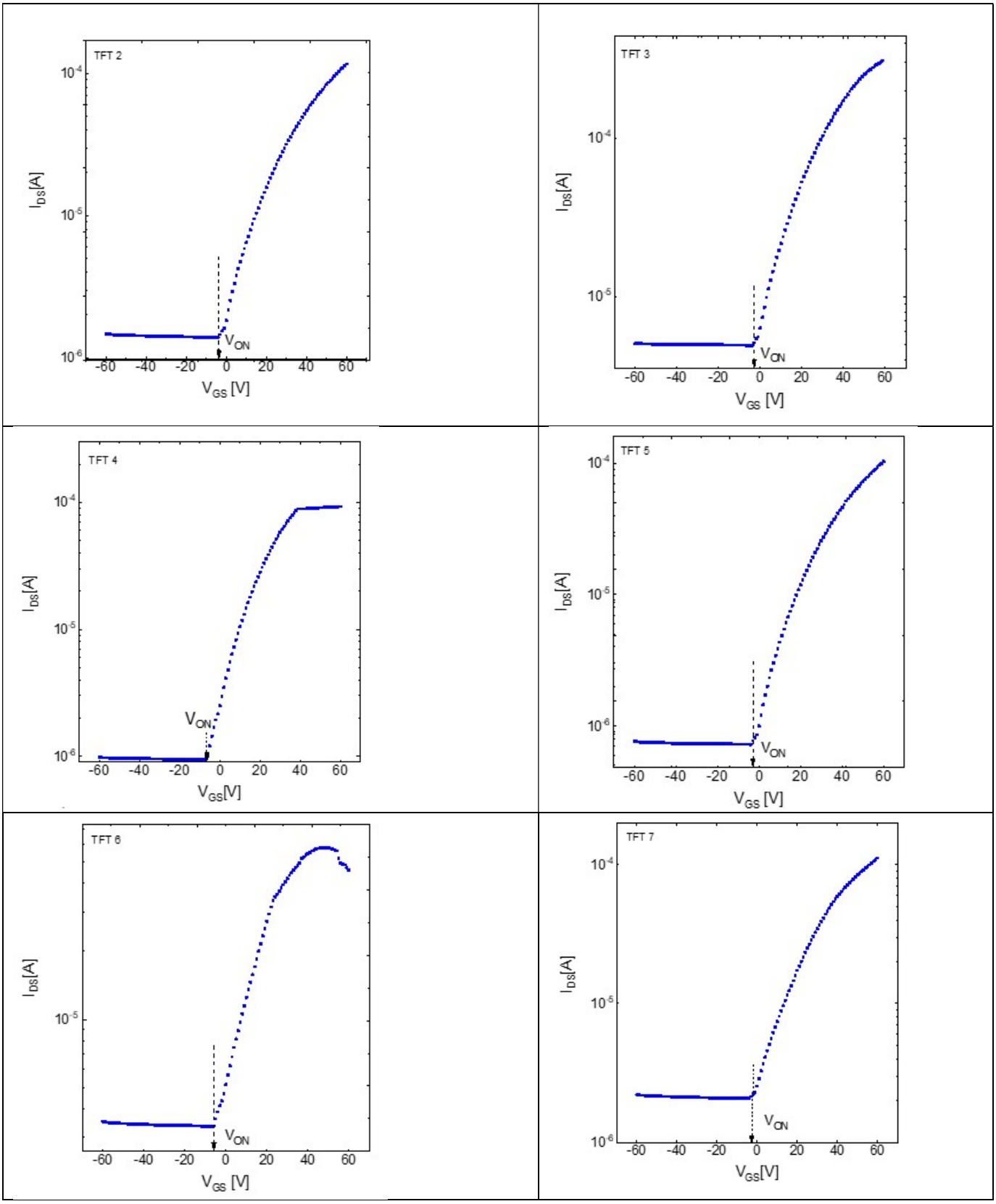
V_{GS}[V]
V_{TH}


TFT 2
TFT 3
TFT 4
TFT 5
TFT 6
TFT 7
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V_{GS} [V]
V_{ON}
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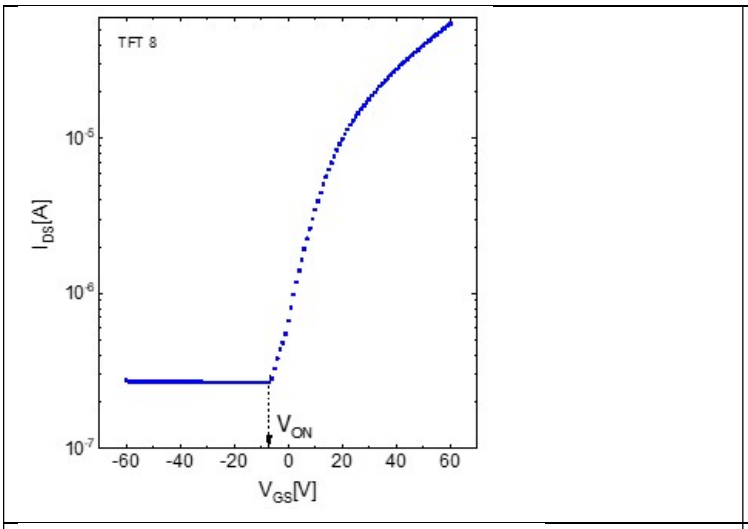
10^{-6}
-60 -40 -20 0 20 40 60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10^{-7}
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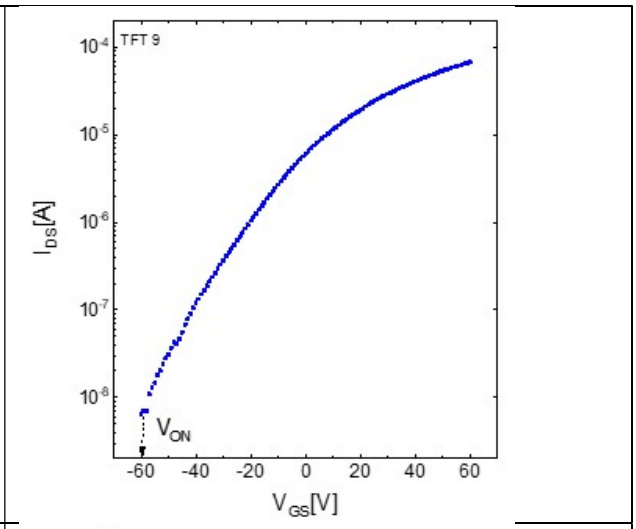
V_{GS}[V]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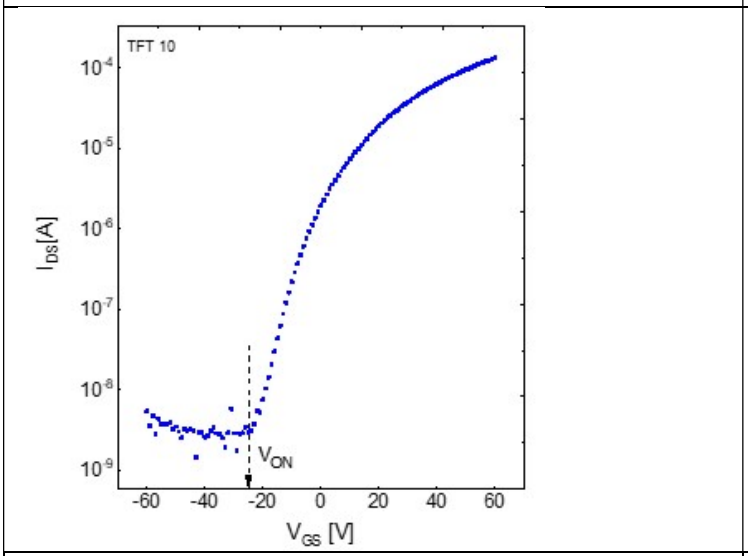
V_{GS}[V]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V_{ON}
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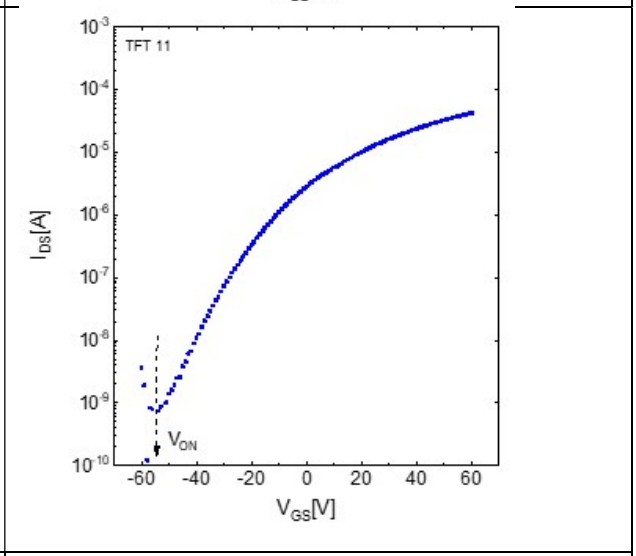
V_{GS} [V]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V_{ON}
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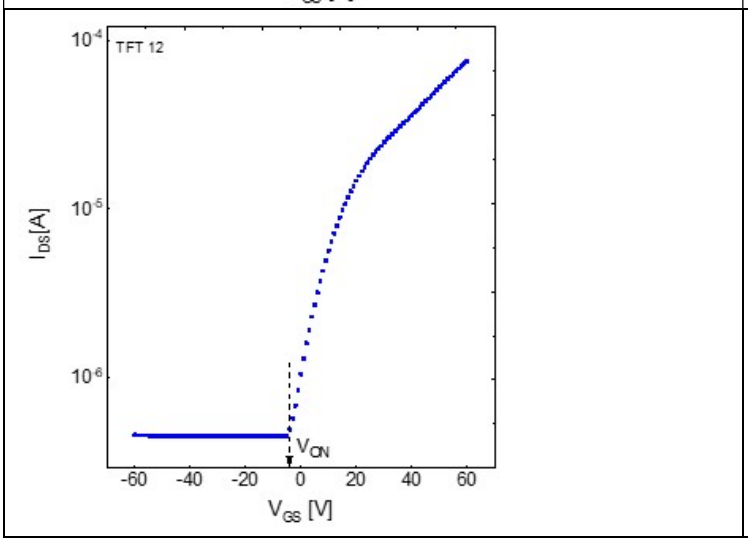
V_{GS}[V]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V_{ON}
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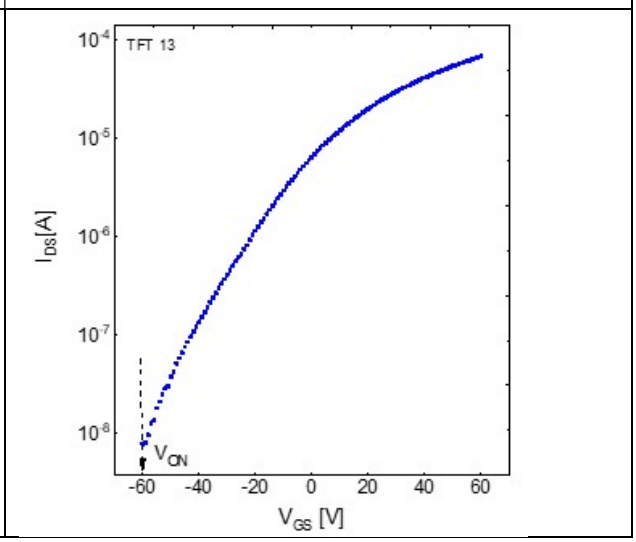
V_{GS} [V]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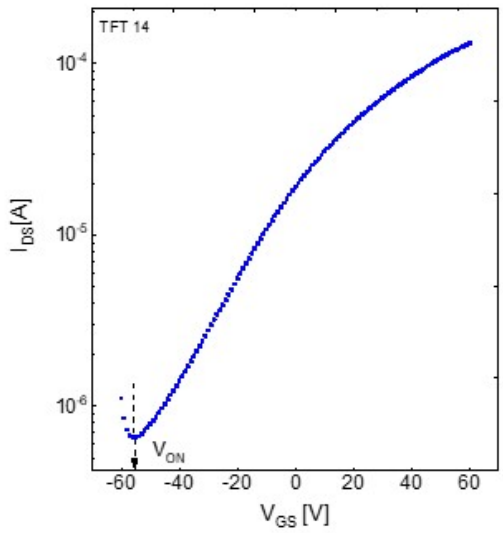
V_{GS} [V]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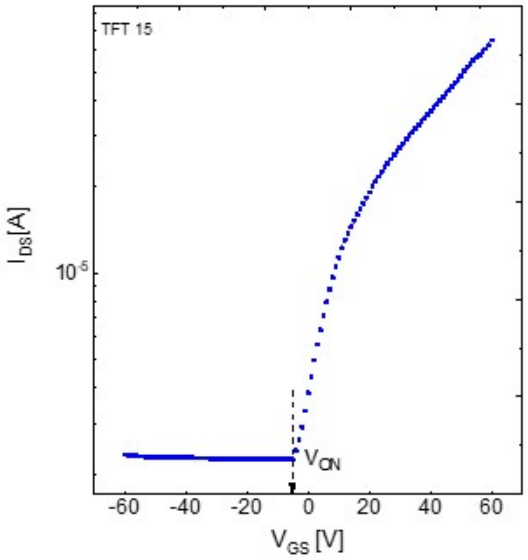
V_{GS} [V]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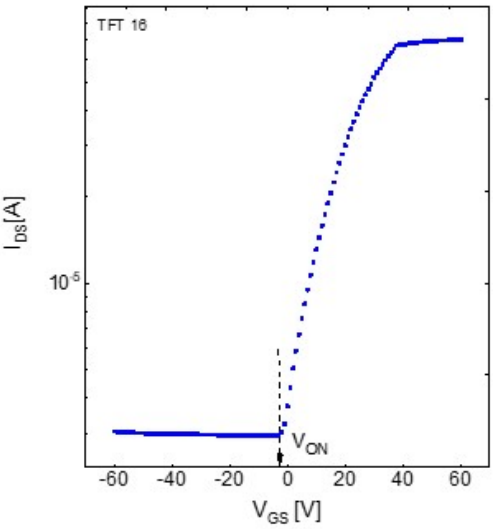
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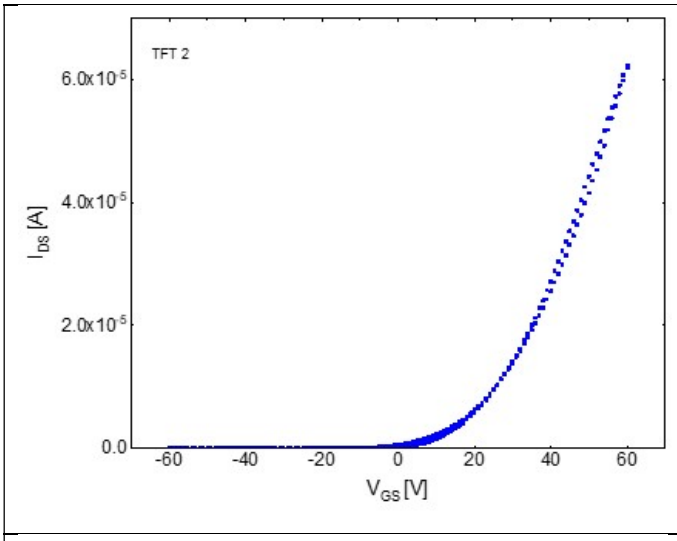
V_{GS} [V]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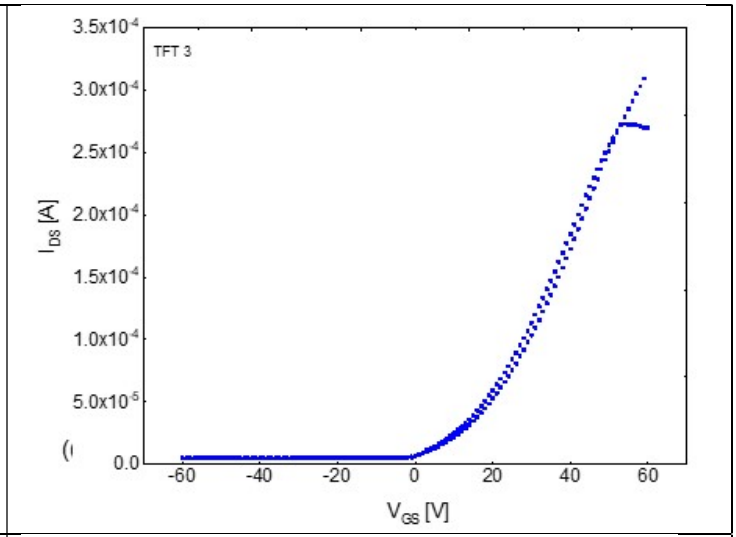
VGS [V]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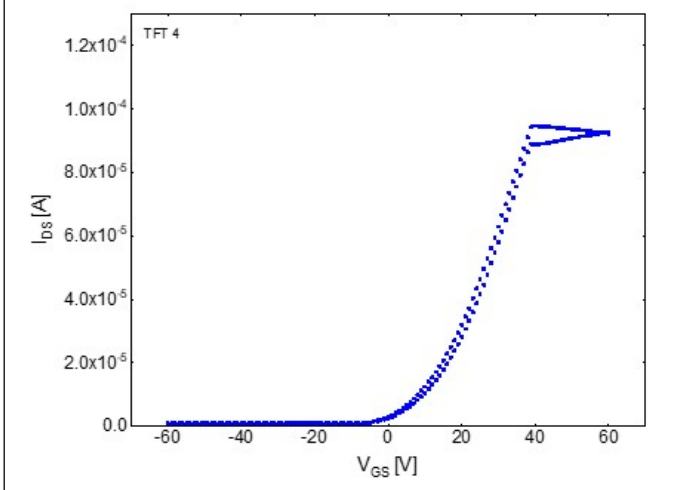
VGS [V]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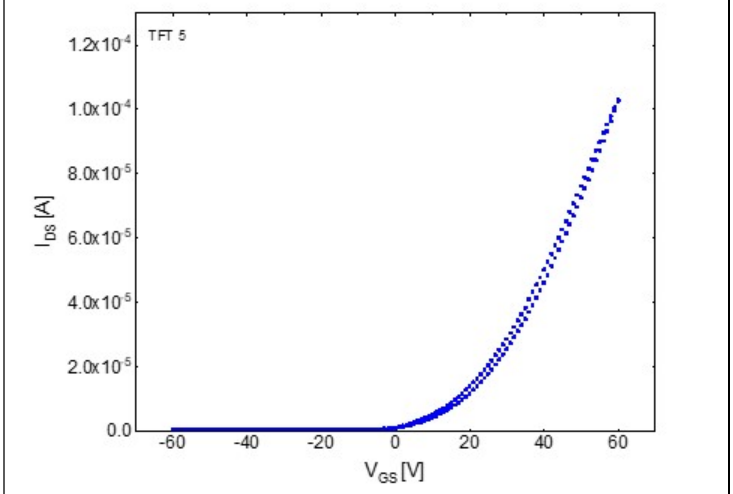
VGS [V]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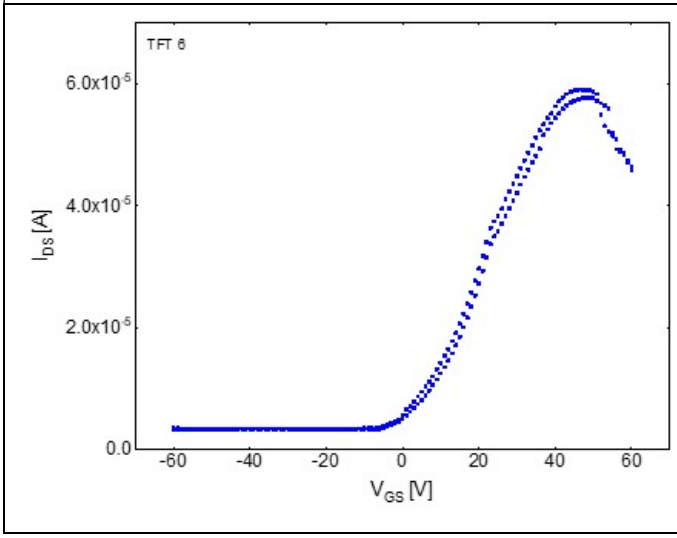
20
40
60
VGS [V]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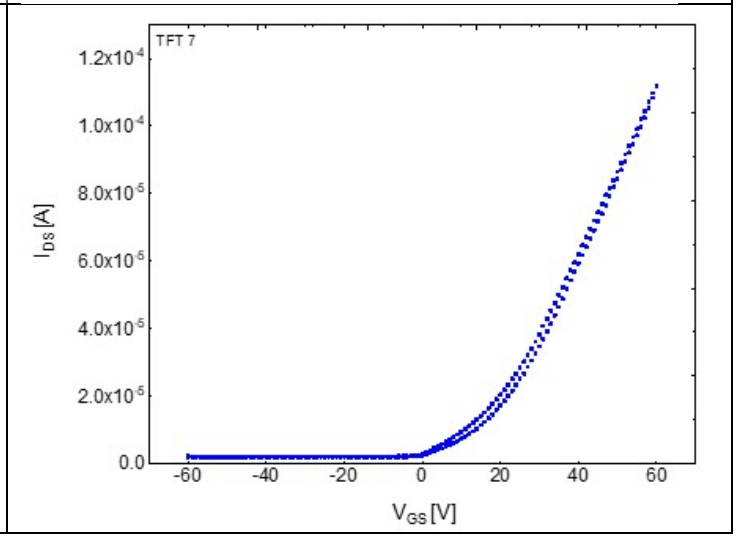
VGS [V]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6.0x10-5
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2.0x10-5
0.0
IDS [A]
-60
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-20
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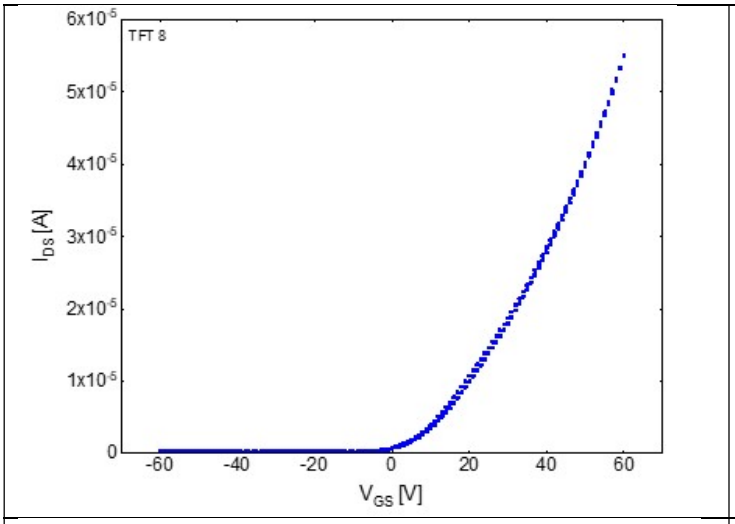
20
40
60
VGS [V]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6x10-5
5x10-5
4x10-5
3x10-5
2x10-5
1x10-5
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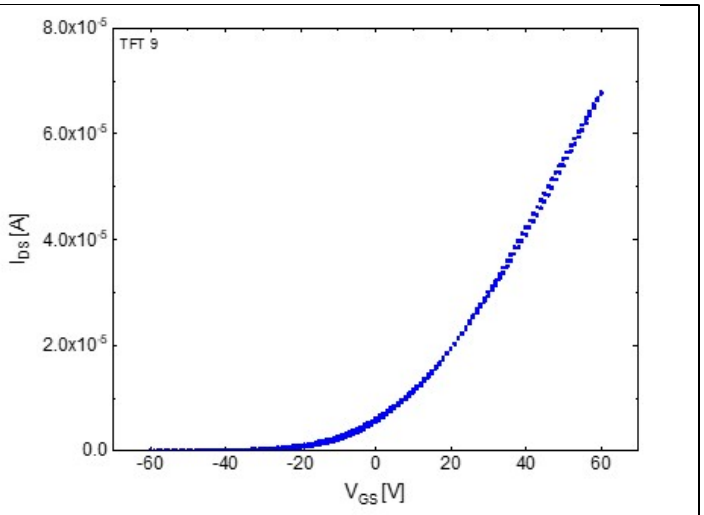
-40
-20
0
20
40
60
VGS [V]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6.0x10-5
4.0x10-5
2.0x10-5
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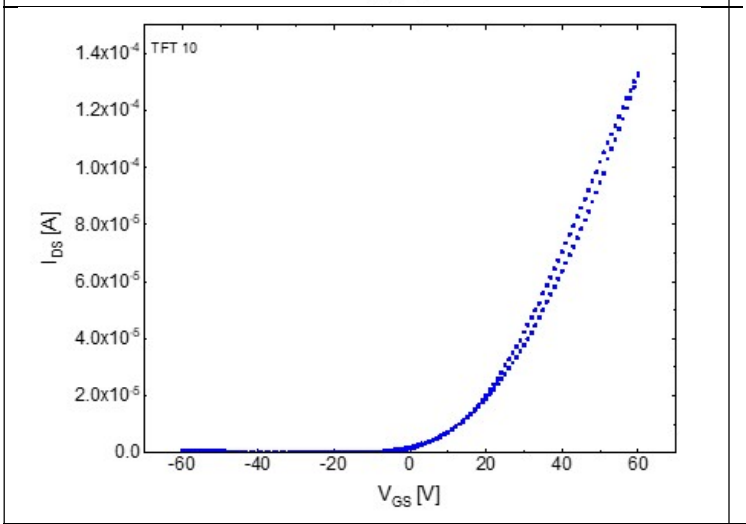
-20
0
20
40
60
VGS [V]


TFT 10
1.4x10-4
1.2x10-4
1.0x10-4
8.0x10-5
6.0x10-5
4.0x10-5
2.0x10-5
0.0
IDS [A]
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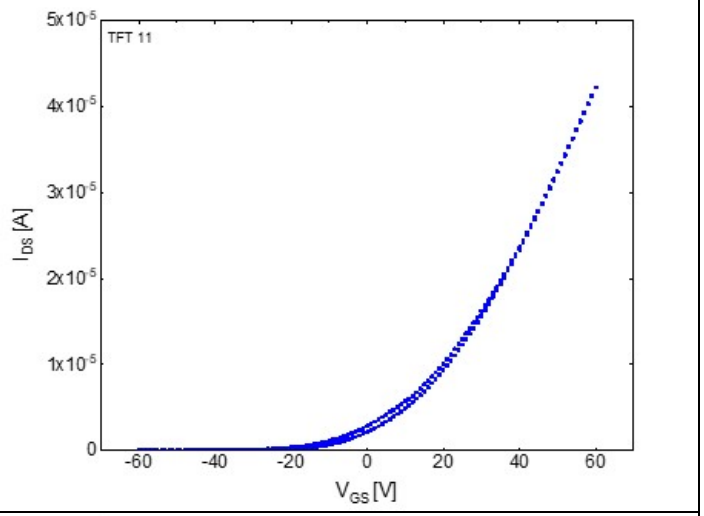
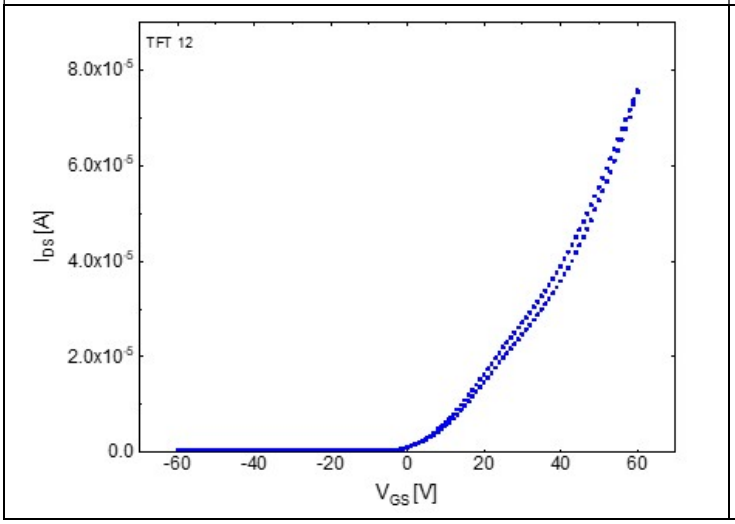
-40
-20
0
20
40
60
VGS [V]


TFT 11
5x10-5
4x10-5
3x10-5
2x10-5
1x10-5
0
IDS [A]
-60
-40
-20
0
20
40
60
VGS [V]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8.0x10-5
6.0x10-5
4.0x10-5
2.0x10-5
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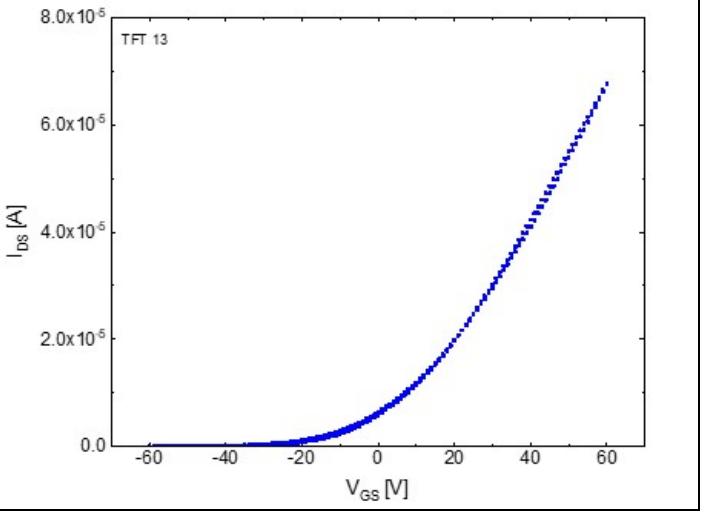
IDS [A]
-60
-40
-20
0
20
40
60
VGS [V]


TFT 13
8.0x10-5
6.0x10-5
4.0x10-5
2.0x10-5
0.0
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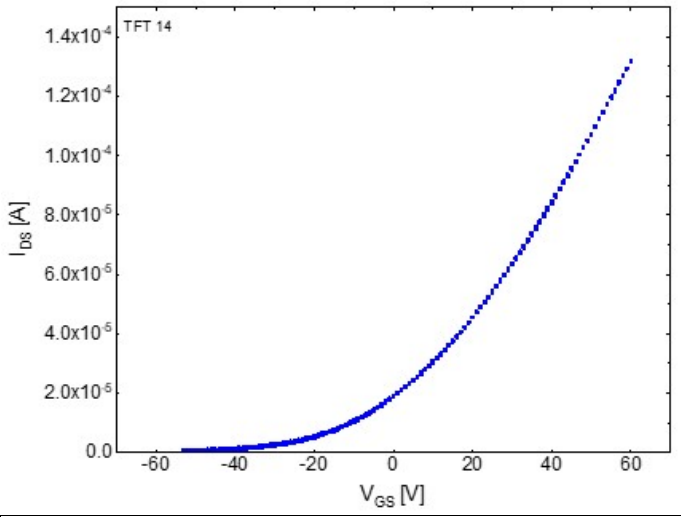
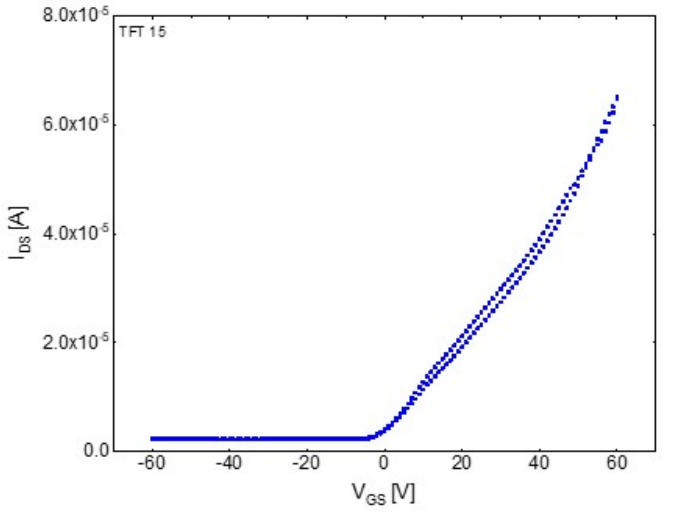
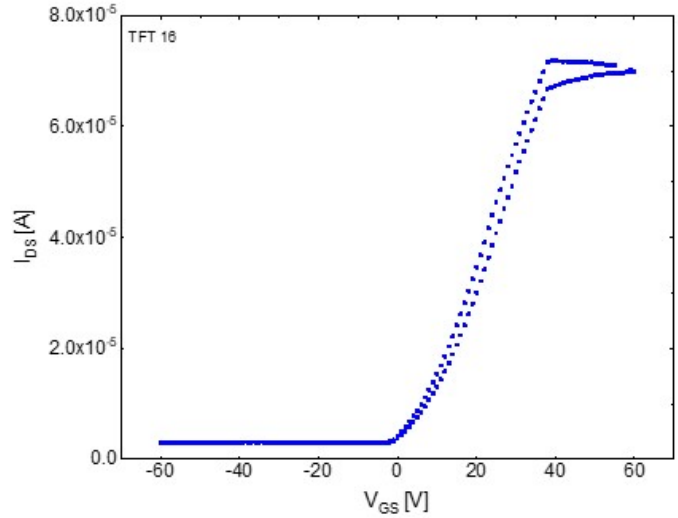
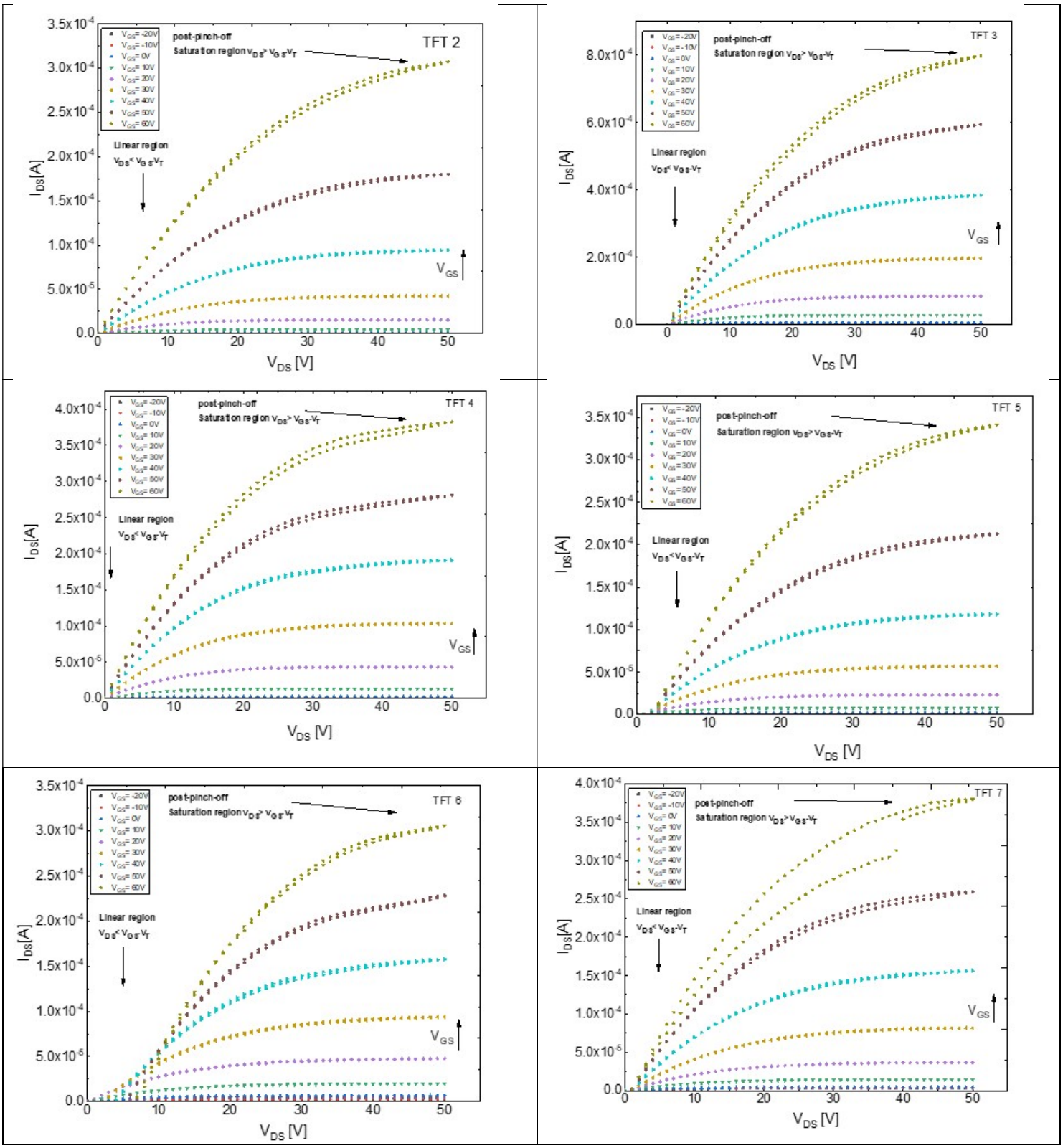
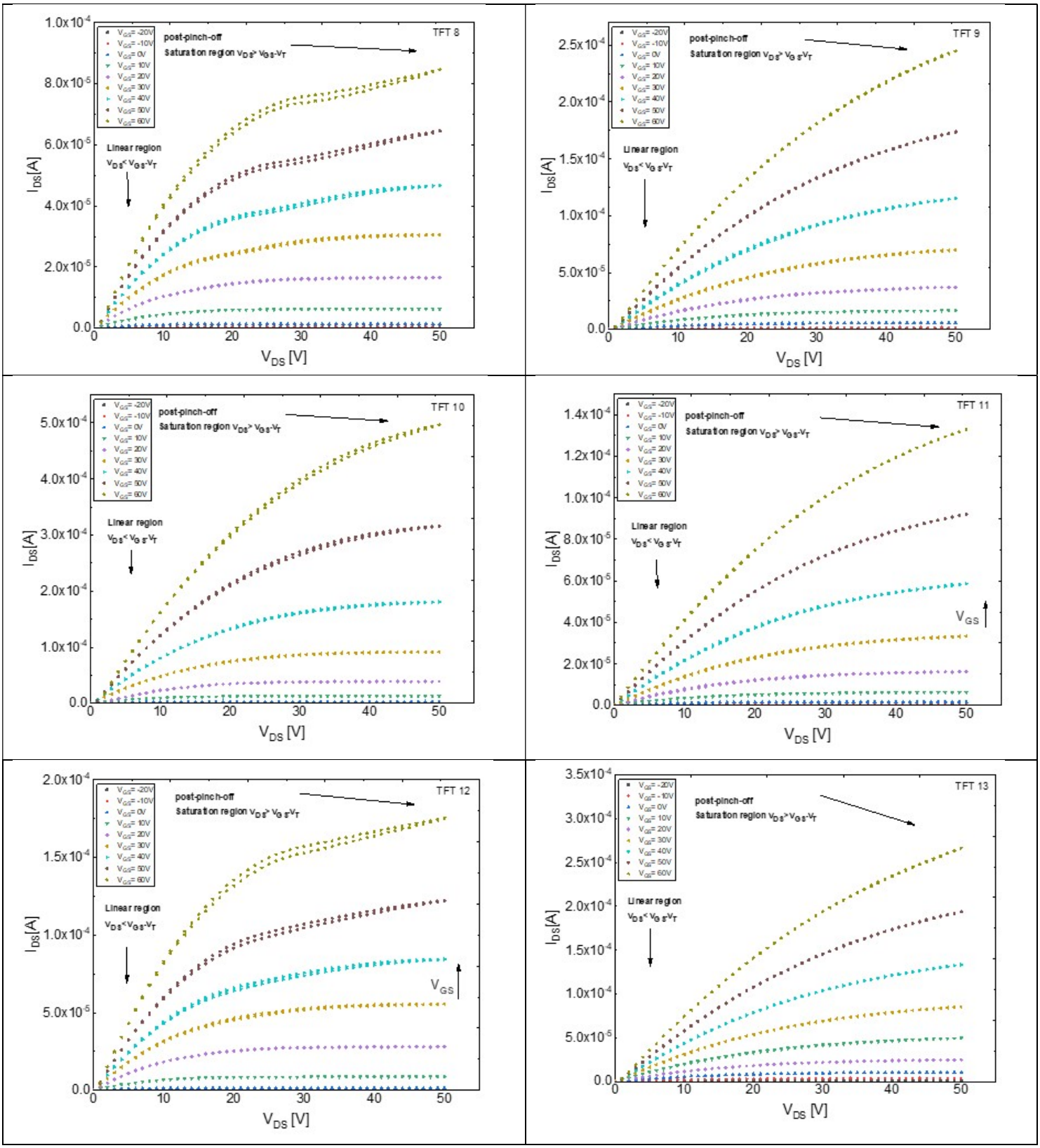
-60
-40
-20
0
20
40
60
VGS [V]

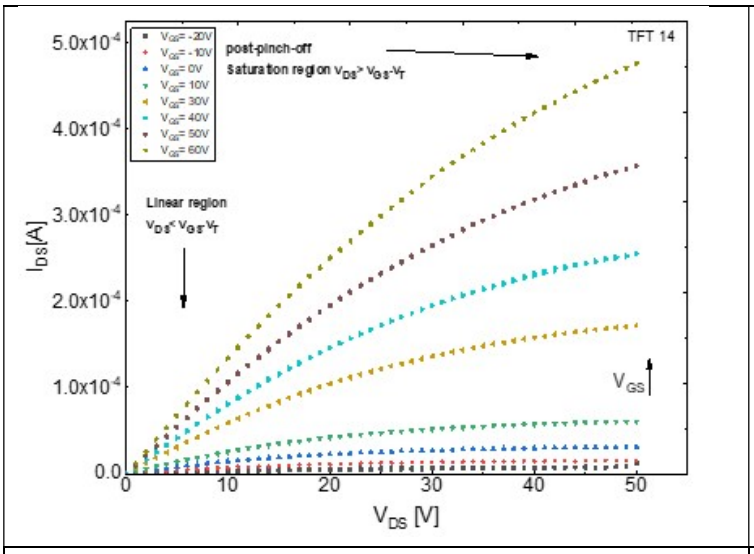

TFT 14
1.4x10-4
1.2x10-4
1.0x10-4
8.0x10-5
6.0x10-5
4.0x10-5
2.0x10-5
0.0
IDS [A]
-60
-40
-20
0
20
40
60
VGS [V]

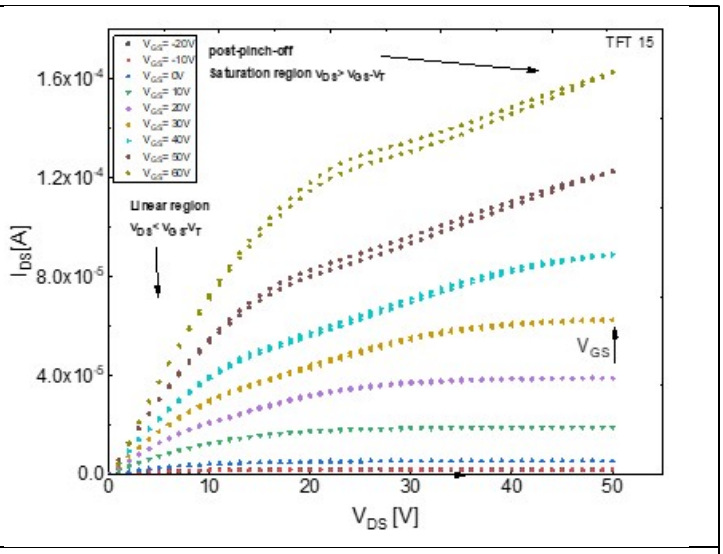

TFT 15
8.0x10-5
6.0x10-5
4.0x10-5
2.0x10-5
0.0
IDS [A]
-60
-40
-20
0
20
40
60
VGS [V]

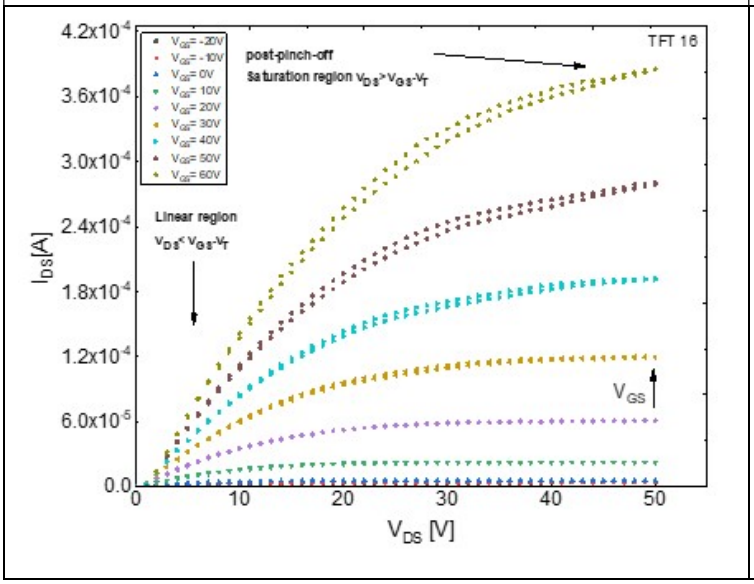

TFT 16
8.0x10-5
6.0x10-5
4.0x10-5
2.0x10-5
0.0
IDS [A]
-60
-40
-20
0
20
40
60
VGS [V]

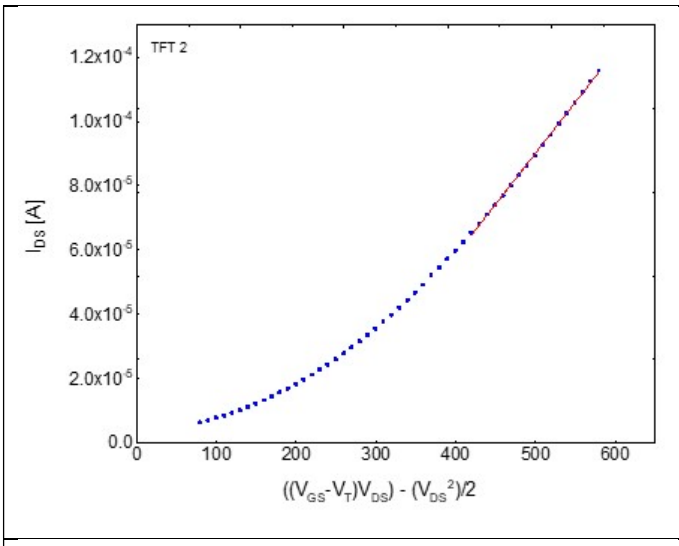

TFT 2
post-pinch-off
Saturation region $V_{DS}>V_{GS}-V_T$
Linear region
$V_{DS}<V_{GS}-V_T$
V_{GS}
I_{DS}[A]
V_{DS} [V]
TFT 3
post-pinch-off
Saturation region $V_{DS}>V_{GS}-V_T$
Linear region
$V_{DS}<V_{GS}-V_T$
V_{GS}
I_{DS}[A]
V_{DS} [V]
TFT 4
post-pinch-off
Saturation region $V_{DS}>V_{GS}-V_T$
Linear region
$V_{DS}<V_{GS}-V_T$
V_{GS}
I_{DS}[A]
V_{DS} [V]
TFT 5
post-pinch-off
Saturation region $V_{DS}>V_{GS}-V_T$
Linear region
$V_{DS}<V_{GS}-V_T$
I_{DS}[A]
V_{DS} [V]
TFT 6
post-pinch-off
Saturation region $V_{DS}>V_{GS}-V_T$
Linear region
$V_{DS}<V_{GS}-V_T$
V_{GS}
I_{DS}[A]
V_{DS} [V]
TFT 7
post-pinch-off
Saturation region $V_{DS}>V_{GS}-V_T$
Linear region
$V_{DS}<V_{GS}-V_T$
V_{GS}
I_{DS}[A]
V_{DS} [V]

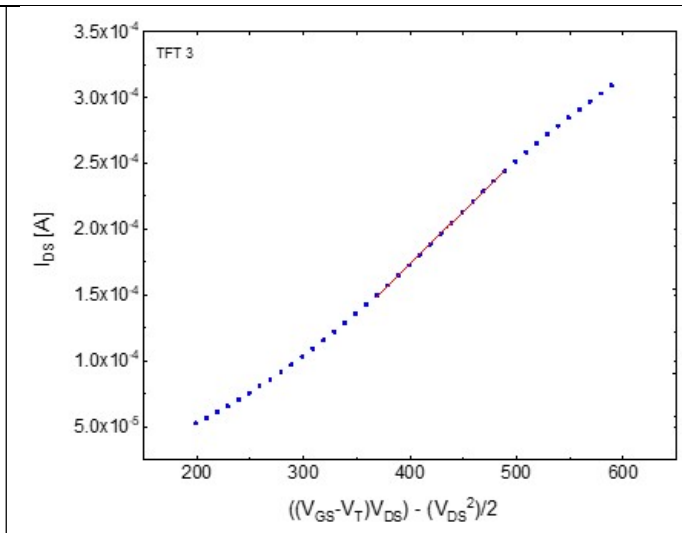

TFT 8
post-pinch-off
Saturation region $V_{DS}> V_{GS}-V_T$
Linear region
$V_{DS}< V_{GS}-V_T$
V_{GS}= -20V
V_{GS}= -10V
V_{GS}= 0V
V_{GS}= 10V
V_{GS}= 20V
V_{GS}= 30V
V_{GS}= 40V
V_{GS}= 50V
V_{GS}= 60V
I_{DS}[A]
V_{DS} [V]
TFT 9
post-pinch-off
Saturation region $V_{DS}> V_{GS}-V_T$
Linear region
$V_{DS}< V_{GS}-V_T$
I_{DS}[A]
V_{DS} [V]
TFT 10
post-pinch-off
Saturation region $V_{DS}> V_{GS}-V_T$
Linear region
$V_{DS}< V_{GS}-V_T$
I_{DS}[A]
V_{DS} [V]
TFT 11
post-pinch-off
Saturation region $V_{DS}> V_{GS}-V_T$
Linear region
$V_{DS}< V_{GS}-V_T$
V_{GS}
I_{DS}[A]
V_{DS} [V]
TFT 12
post-pinch-off
Saturation region $V_{DS}> V_{GS}-V_T$
Linear region
$V_{DS}< V_{GS}-V_T$
V_{GS}
I_{DS}[A]
V_{DS} [V]
TFT 13
post-pinch-off
Saturation region $V_{DS}> V_{GS}-V_T$
Linear region
$V_{DS}< V_{GS}-V_T$
I_{DS}[A]
V_{DS} [V]

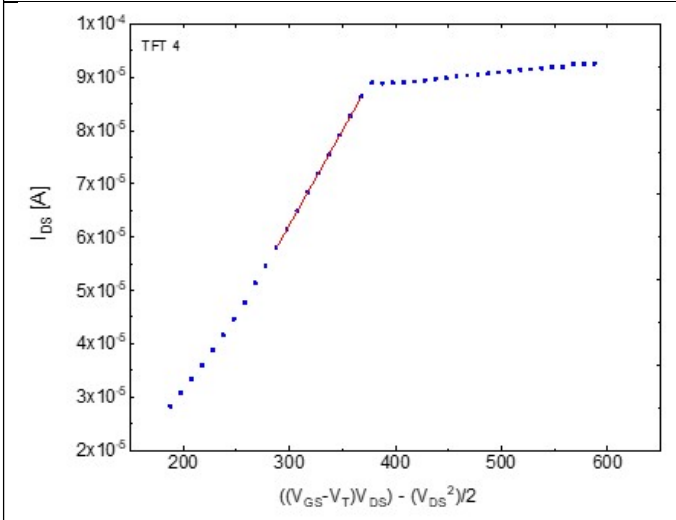

TFT 14
post-pinch-off
Saturation region $V_{DS} > V_{GS}-V_T$
Linear region
$V_{DS} < V_{GS}-V_T$
V_{GS}
I_{DS}[A]
V_{DS} [V]
V_{GS}= -20V
V_{GS}= -10V
V_{GS}= 0V
V_{GS}= 10V
V_{GS}= 30V
V_{GS}= 40V
V_{GS}= 50V
V_{GS}= 60V
5.0x10^{-4}
4.0x10^{-4}
3.0x10^{-4}
2.0x10^{-4}
1.0x10^{-4}
0.0
0
10
20
30
40
50

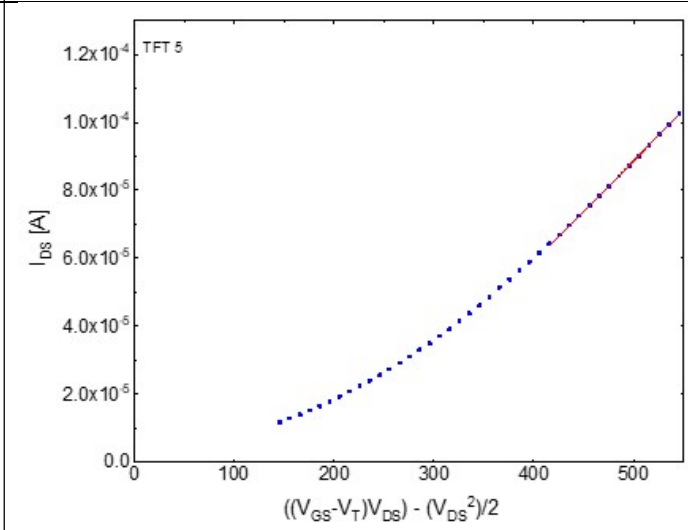

TFT 15
post-pinch-off
Saturation region $V_{DS} > V_{GS}-V_T$
Linear region
$V_{DS} < V_{GS}-V_T$
V_{GS}
I_{DS}[A]
V_{DS} [V]
V_{GS}= -20V
V_{GS}= -10V
V_{GS}= 0V
V_{GS}= 10V
V_{GS}= 20V
V_{GS}= 30V
V_{GS}= 40V
V_{GS}= 50V
V_{GS}= 60V
1.6x10^{-4}
1.2x10^{-4}
8.0x10^{-5}
4.0x10^{-5}
0.0
0
10
20
30
40
50

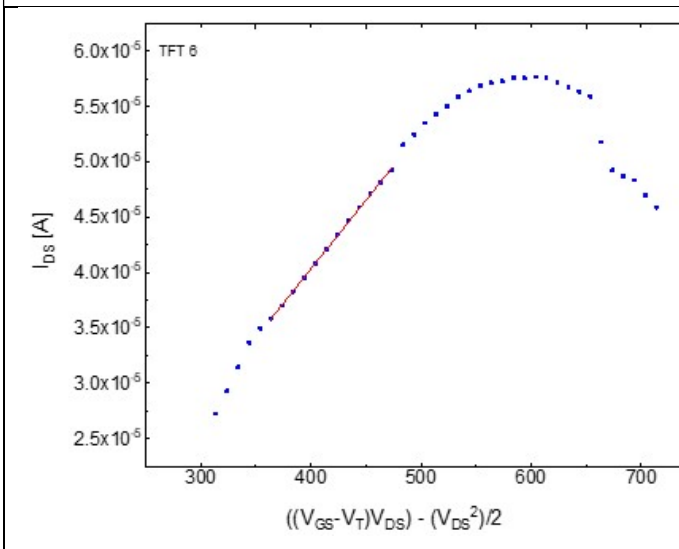

TFT 16
post-pinch-off
Saturation region $V_{DS} > V_{GS}-V_T$
Linear region
$V_{DS} < V_{GS}-V_T$
V_{GS}
I_{DS}[A]
V_{DS} [V]
V_{GS}= -20V
V_{GS}= -10V
V_{GS}= 0V
V_{GS}= 10V
V_{GS}= 20V
V_{GS}= 30V
V_{GS}= 40V
V_{GS}= 50V
V_{GS}= 60V
4.2x10^{-4}
3.6x10^{-4}
3.0x10^{-4}
2.4x10^{-4}
1.8x10^{-4}
1.2x10^{-4}
6.0x10^{-5}
0.0
0
10
20
30
40
50

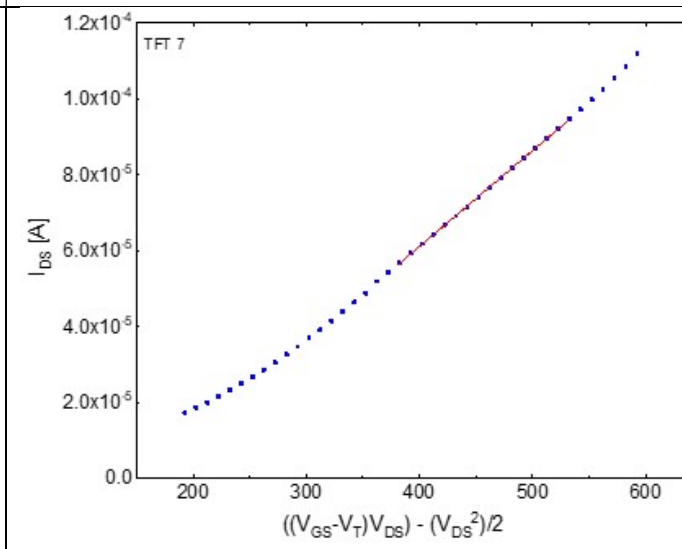

TFT 2
I_{DS} [A]
$((V_{GS}-V_T)V_{DS}) - (V_{DS}^2)/2$

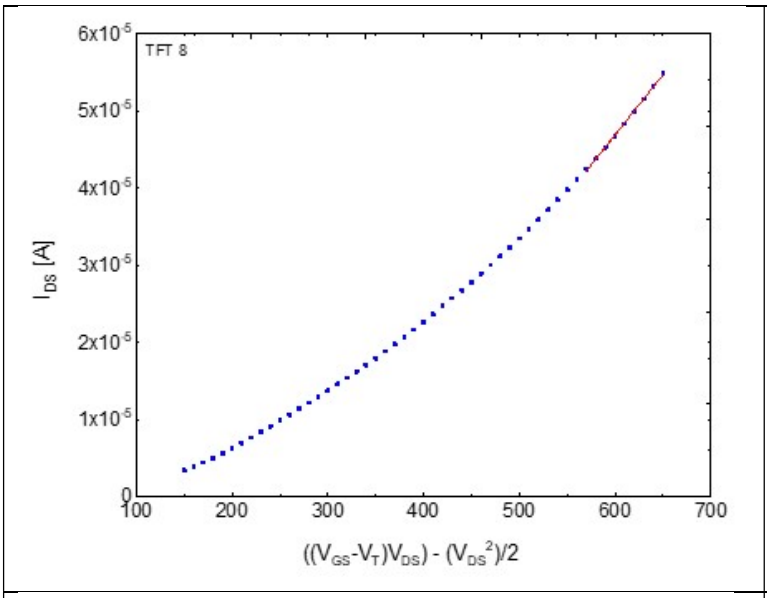

TFT 3
I_{DS} [A]
$((V_{GS}-V_T)V_{DS}) - (V_{DS}^2)/2$

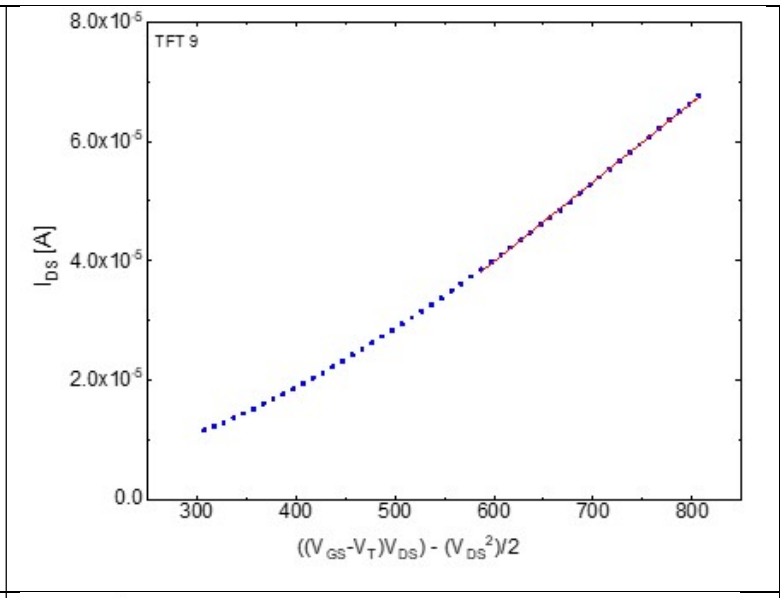

TFT 4
I_{DS} [A]
$((V_{GS}-V_T)V_{DS}) - (V_{DS}^2)/2$

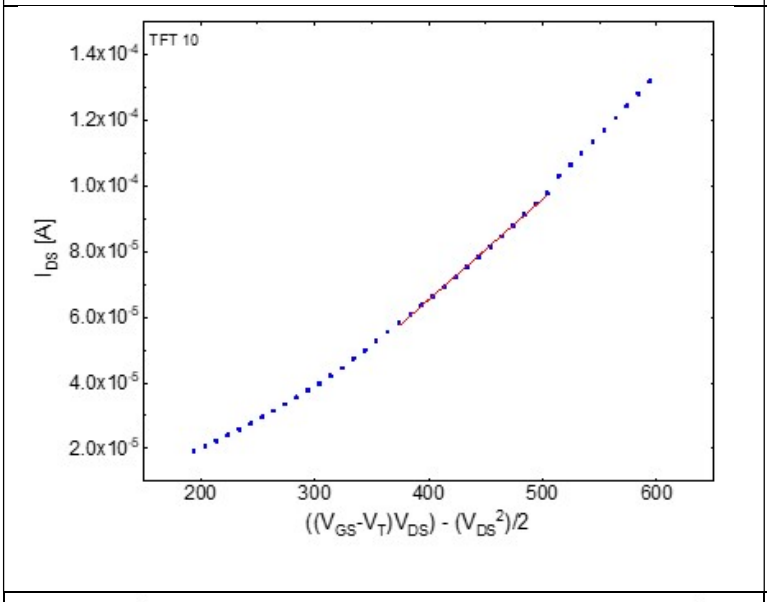

TFT 5
I_{DS} [A]
$((V_{GS}-V_T)V_{DS}) - (V_{DS}^2)/2$

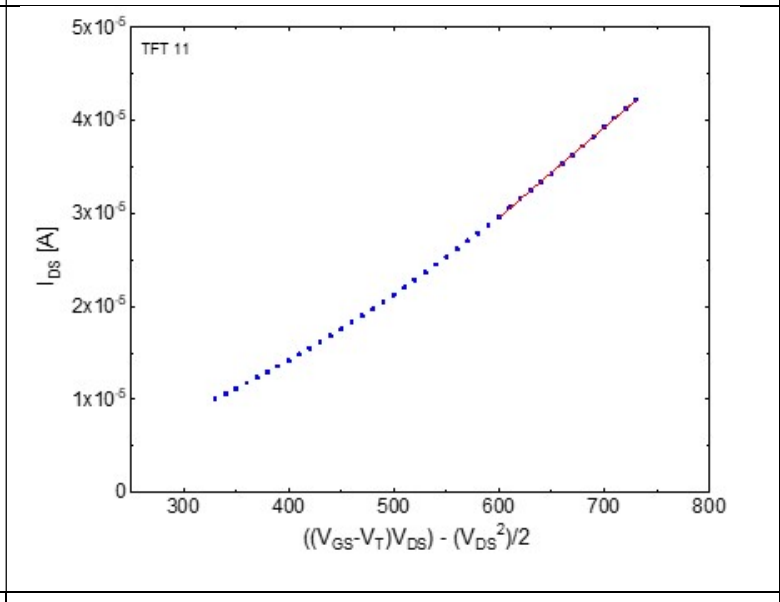

TFT 6
I_{DS} [A]
$((V_{GS}-V_T)V_{DS}) - (V_{DS}^2)/2$

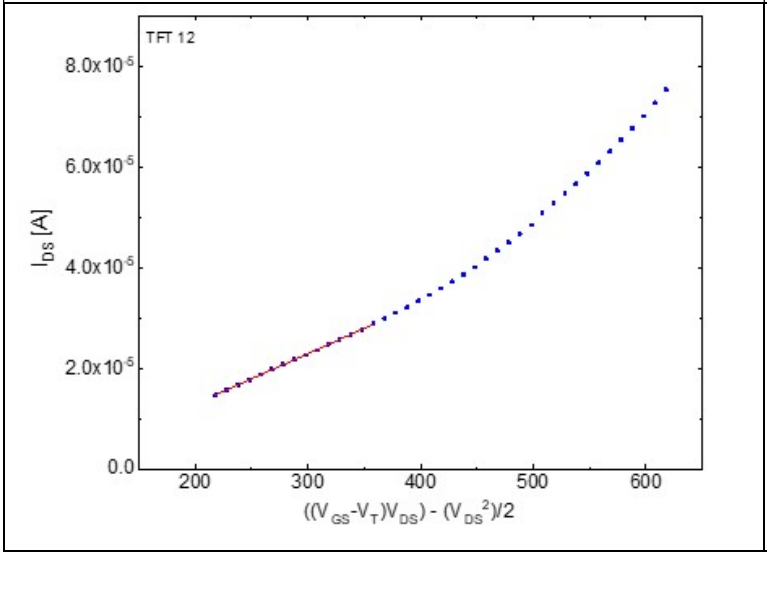

TFT 7
I_{DS} [A]
$((V_{GS}-V_T)V_{DS}) - (V_{DS}^2)/2$

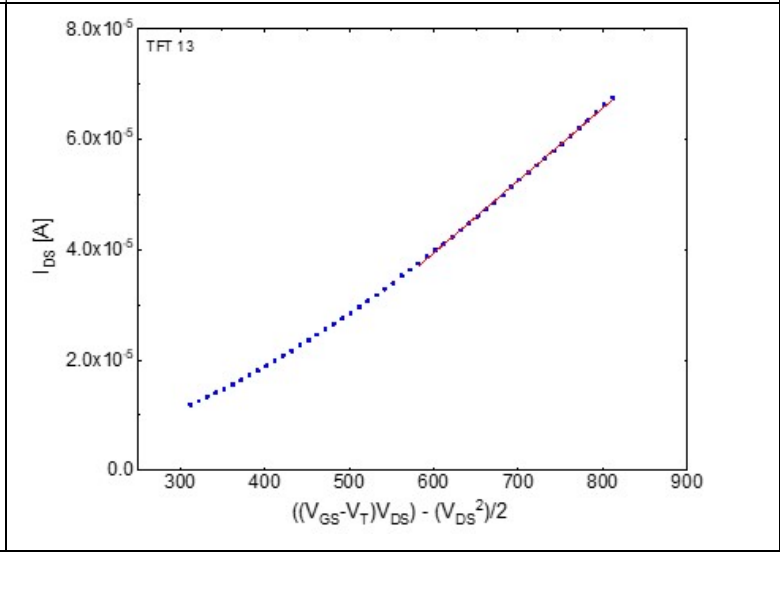

TFT 8
I_{DS} [A]
$((V_{GS}-V_T)V_{DS}) - (V_{DS}^2)/2$

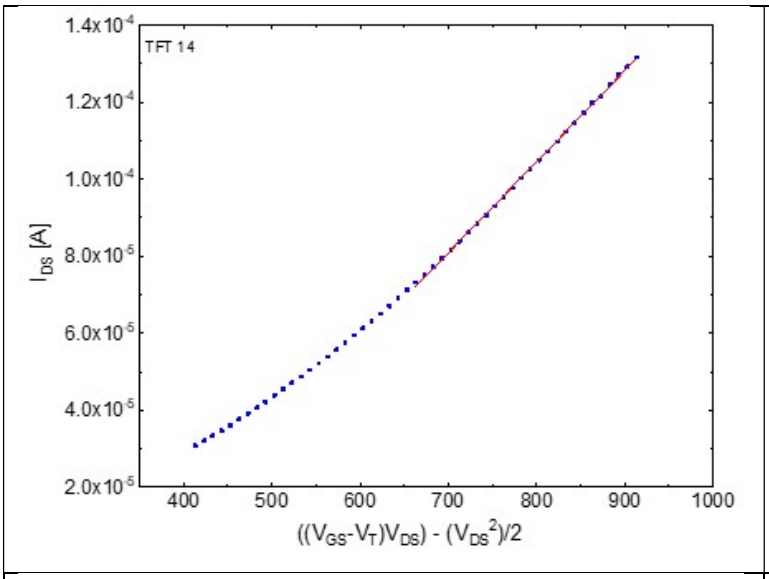

TFT 9
I_{DS} [A]
$((V_{GS}-V_T)V_{DS}) - (V_{DS}^2)/2$

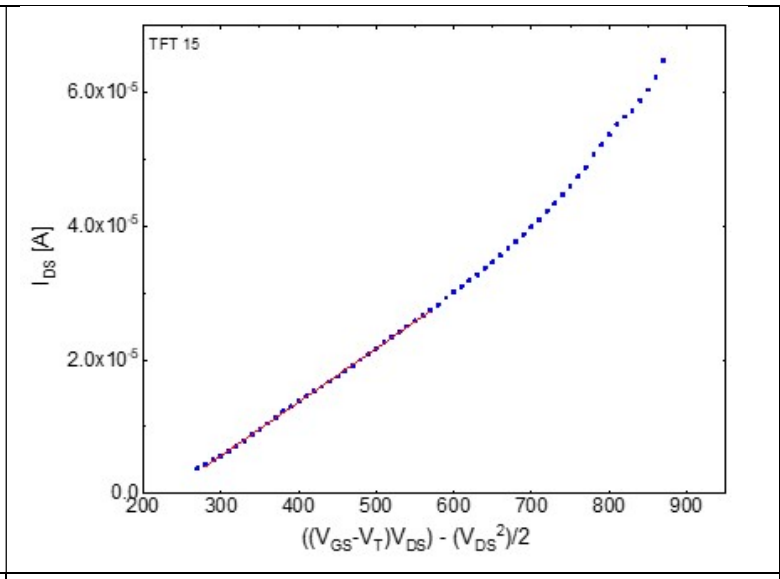

TFT 10
I_{DS} [A]
$((V_{GS}-V_T)V_{DS}) - (V_{DS}^2)/2$

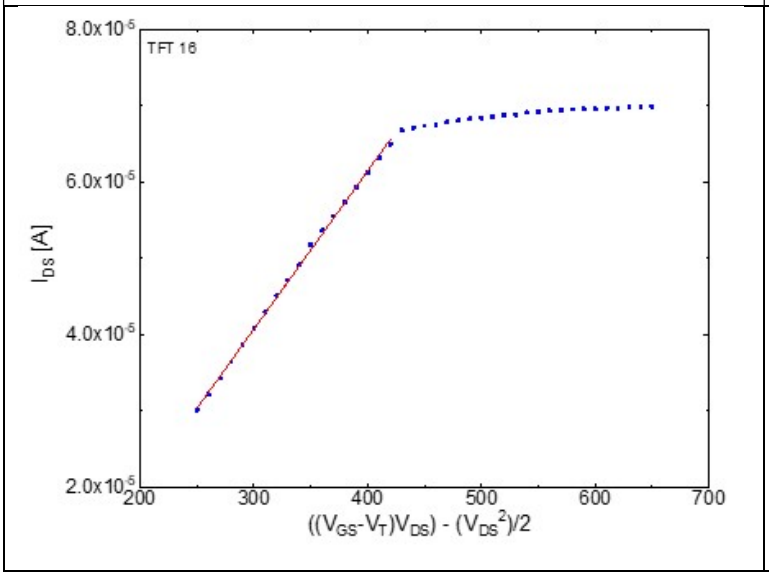

TFT 11
I_{DS} [A]
$((V_{GS}-V_T)V_{DS}) - (V_{DS}^2)/2$


TFT 12
I_{DS} [A]
$((V_{GS}-V_T)V_{DS}) - (V_{DS}^2)/2$


TFT 13
I_{DS} [A]
$((V_{GS}-V_T)V_{DS}) - (V_{DS}^2)/2$


TFT 14
1.4x10-4
1.2x10-4
1.0x10-4
8.0x10-5
6.0x10-5
4.0x10-5
2.0x10-5
IDS [A]
400
500
600
700
800
900
1000
((VGS-VT)VDS) - (VDS2)/2


TFT 15
6.0x10-5
4.0x10-5
2.0x10-5
0.0
IDS [A]
200
300
400
500
600
700
800
900
((VGS-VT)VDS) - (VDS2)/2


TFT 16
8.0x10-5
6.0x10-5
4.0x10-5
2.0x10-5
IDS [A]
200
300
400
500
600
700
((VGS-VT)VDS) - (VDS2)/2

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