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Fermi-level pinning and charge neutrality level in germanium

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The Schottky barrier height in metal/Ge contacts shows weak dependence on the metal work function indicating strong Fermi-level pinning close to the Bardeen limit. The pinning factor S is about 0.05 and the charge neutrality level (CNL) is only about 0.09 eV above the top of the valence band. Because of this, the Fermi level in Ge lies higher than CNL in most cases of interest so that unpassivated acceptorlike gap states at the interface are easily filled, building up a *net negative* fixed charge. This could prevent efficient inversion of a p-type Ge surface in a metal-oxide-semiconductor structure. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2410241]

Schottky contacts between metals and semiconductors have been the subject of research for many years.[1] Most of the work focuses on Si, III-V, and other compound semiconductors because of their technological importance. Considerably less is known about Schottky contacts on Ge. The interest in this material has increased significantly since the first demonstration[2] of functional metal-oxide-semiconductor field-effect transistors (MOSFETs) with high-k gate dielectrics. This has opened the possibility to enhance the high frequency performance of digital logic devices taking advantage of the higher carrier mobilities in Ge. Despite significant progress in Ge p-channel transistors,[2–7] the n-channel MOSFETs are barely functional, often exhibiting low channel mobility[9,10] and ON-state currents.[7–10] The importance of substrate doping in improving channel mobility in Ge nMOSFETs has been recognized recently;[11] however the reasons for the inferior performance frequently observed in n-channel devices are not fully understood at the present time. The Ge p-n junctions present also a big challenge because they have high leakage as a result of the small energy gap. In addition, dopants in Ge present low solid solubility,[12] incomplete activation, and enhanced diffusion,[12] which result in poor quality source-drain (S/D) contacts inducing high OFF-and low ON-state currents. This has triggered research in Shottky barrier S/D transistors[13–15] with the aim to improve the dc characteristics.

Apart from the technological importance, there is also scientific interest. Metal/Ge contacts offer the possibility to study fundamental properties of interfaces such as the Fermi-level pinning and the charge neutrality level (CNL), which are largely unknown for Ge. In early works[16,17] the focus was mainly on the pinning factor S for which values of 0.4 (Ref. 16) and 0.02 (Ref. 17) were obtained. These differ between each other significantly, so that a conclusion about the strength of Fermi-level pinning could not be made. In addition, apart from theoretical calculations,[18,19] no experimental evidence is available for the CNL of Ge.

Here, we measure the pinning factor and the CNL in Ge using Schottky diodes with a variety of metals. We also discuss the possible influence of the CNL on inverting the surface of p-type Ge in an attempt to understand the frequently observed poor performance of Ge nMOSFET devices.

The Schottky diodes were made on phosphorus-doped n-type Ge substrates using shadow masks with a resistivity of 0.027 Ω cm. The native oxide was first desorbed *in situ* in UHV by heating the substrate to 360 °C for 15 min until a (2×1)-reconstructed surface is observed by reflection high energy electron diffraction through large openings in the masks, which is indicative of a clean and flat surface. Subsequently, 30-nm-thick metals were deposited *in situ* at room temperature. In the case of reactive metals (e.g., Ce, La, Hf, etc.), a 30-nm-thick Pt cap layer was deposited without breaking vacuum in order to avoid oxidation. The J-V characteristics for three of the Schottky diodes are shown in Fig. 1. These are modeled according to the equivalent circuit[20] in the inset of Fig. 1 which takes into account series resistance and parasitic leakage effects. On the basis of this circuit, the current as a function of voltage is given by $I=I_d+I_p=I_s(\exp((V-IR_S)/nkT)-1)+G_p(V-IR_S)$. The saturation current I_s in the thermionic emission approximation is given by[21] $I_s=AA^*T^2\exp(-q\Phi_b/kT)$, where

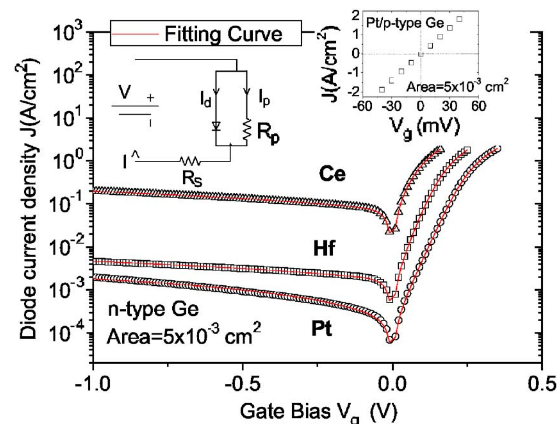

FIG. 1. (Color online) J-V characteristics for three of the metal/n-Ge Schottky diodes. The inset at the upper left shows the equivalent circuit used for the modeling (solid lines). I_d is the current passing through an ideal diode and I_p is the parallel current due to parasitic leakage. The inset at the upper right shows Pt/p-Ge Ohmic contacts.

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TABLE I. Metal/n-Ge Schottky diode parameters.

Metal	Barrier height $\Phi_{b,e}$ (eV)	Ideality factor n	Series resistance R_S (Ω)	Parallel conductance G_P ($S\times10^{-4}$)
Pt	0.64	1.12	8.47	0.08
Hf	0.58	1.04	6.70	0.13
Ni	0.58	1.04	6.45	0.07
Ti	0.57	1.03	6.65	0.22
Ta	0.51	2.12	15.10	10.67
La	0.51	1.04	13.46	0.84
Gd	0.49	1.11	7.40	8.42
Ce	0.49	1.06	8.10	5.99

$A=5\times10^{-3}$ cm^2 is the diode area and $A^*=143$ A/cm^2 K^2 is the Richardson constant[21] for Ge (100).

The barrier height for electrons $\Phi_{b,e}$, the ideality factor n, the series resistance R_s, and the parallel conductance $G_p=1/R_p$ are treated as adjustable parameters and are estimated from the fitting of the experimental curves (see Fig. 1). Their values are listed in Table I. The barrier height as a function of metal work function Φ_m is plotted in Fig. 2, where Φ_m values are taken from Ref. 22. We observe a linear behavior, which is expected since $\Phi_{b,e}$ is given by[23] $\Phi_{b,e}=S(\Phi_m-\Phi_{\text{CNL}})+(\Phi_{\text{CNL}}-\chi_S)$, where $S\equiv\partial\Phi_{b,e}/\partial\Phi_m$ is the pinning factor and χ_S and Φ_{CNL} are the semiconductor electron affinity and the charge neutrality level, respectively, both measured from the vacuum level (see inset of Fig. 2). A linear fitting of the experimental points yields $\Phi_{b,e}=0.05\Phi_m+0.34$ eV represented by the solid curve in Fig. 2. From the above equations we obtain $S=0.05$ (±0.01) and $\Phi_{\text{CNL}}=4.57$ (±0.07) eV. The CNL measured from the top of the valence band is given by $\Phi_0=E_g+\chi_S-\Phi_{\text{CNL}}$ (see inset of Fig. 2) and takes the value of $\Phi_0=0.09$ (±0.07) eV assuming $\chi_S=4$ eV and $E_g=0.66$ eV. The measured Φ_0 in the present work is between the previously reported theoretical values of 0.18 eV (Ref. 18) and 0.03 eV (Ref. 19) for Ge, while it agrees with the latter within the experimental error.

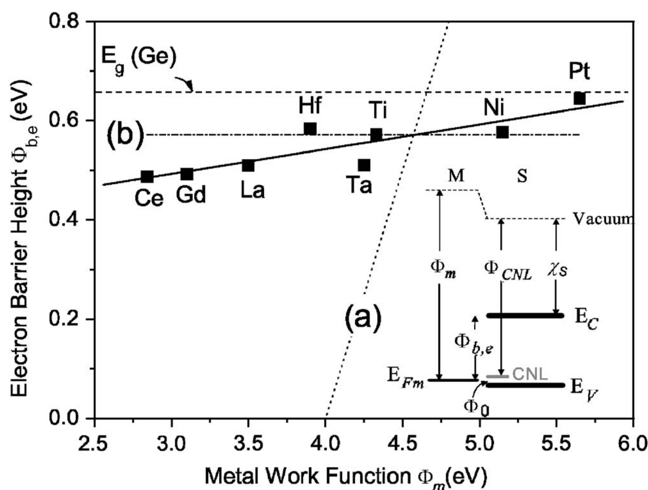

FIG. 2. Barrier height for electrons $\Phi_{b,e}$ vs metal work function Φ_m. The solid line represents a linear fit to the experimental points. The dotted line (a) represents the ideal Schottky limit with $S=1$ and $\Phi_{b,e}=\Phi_m-\chi_S$. The horizontal dash-dotted line (b) represents the Bardeen strong pinning limit with $S=0$ and $\Phi_{b,e}=\Phi_{\text{CNL}}-\chi_S$. The inset shows the alignment of the different energy levels at an arbitrary metal-semiconductor interface.

As seen from Fig. 2 and the extracted value of $S=0.05$, the Schottky barrier is nearly independent from the metal work function falling close to the strong Fermi-level pinning limit (the Bardeen limit) with $S\approx0$. Because of the strong Fermi-level pinning around the CNL [which is only 0.09 eV above the valence band (VB)], all metals give high barrier heights for electrons $\Phi_{b,e}$, close to the Ge band gap E_g (Fig. 2), meaning also that the barrier height for holes $\Phi_{b,h}\approx E_g-\Phi_{b,e}$ is very small (in the case of Pt, $\Phi_{b,h}$ is only 20 meV). As shown in the inset of Fig. 1, Pt on p-type Ge gives ohmic contacts as a result of low $\Phi_{b,h}$, and the same is true for all other metals, implying that they are suitable for pMOSFETs. On the other hand, the same data in Fig. 2 show that it will be hard to find elemental metals with low enough barrier height for electrons. It should be noted, however, that Ti germanides[24] and sulfur-passivated Ni germanide[25] Schottky contacts give $\Phi_{b,e}$ values as low as 0.34 and 0.15 eV, respectively. The latter value of 0.15 eV (Ref. 25) is promising result toward realizing Ohmic contacts on n-type Ge, suitable for nMOSFETs.

The location of CNL close to the valence band (less than 0.1 eV from the top) deserves better attention because it may be related to the frequently observed[7–10] poor performance of nMOSFETs. Attempting a detailed description, we first note that in the virtual induced gap states approximation,[26] exponentially decaying interface states fill the semiconductor gap as a result of the disruption of periodicity at the interface. These are generally a mixture of acceptorlike conduction band (CB) and donorlike VB states[26] with CNL marking the crossing point at which their densities are equal (see Fig. 3). CNL is considered to be mainly a property of the semiconductor itself;[18,26,27] therefore in a first approximation, we may ignore the presence of the insulator and focus on the semiconductor (Fig. 3). The asymmetrical distribution of the density of interface states as depicted in Fig. 3 originates from the lower VB effective density of states in Ge and it is compatible with the position of the CNL close to the VB since CNL is the weighted average[23] of the density of states. The larger density of occupied acceptor states in the upper half of the band gap (also confirmed by other measurements[28]) could cause enhanced Coulomb scattering of electrons in n-channel devices, thus explaining[28,29] the asymmetry[8–10,28,29] in degradation between functional pFETs and nFETs with comparable performance. However, it cannot explain satisfactorily the fact that in several cases the n-channel devices are nonfunctional[5] or severely underperformant[6] despite the use of advanced passivation methodologies[6] which, notably, improve pMOSFET performance.[6] In what follows we attempt to explain this dramatic degradation of nMOSFETs which often results in complete failure. Without loss of generality, we take a typical case of p-type Ge, with a doping $N_A\sim10^{17}$ cm^{-3}. If there is no bias at the gate, the semiconductor Fermi level E_F is aligned with the CNL so that the interface is neutral [Fig. 3(a)]. Applying a positive bias on the gate, the bands bend downwards, drawing CNL away from E_F as illustrated in Fig. 3(b). This is energetically unfavorable though since it creates charge imbalance. Indeed, in this case, more (unpassivated) acceptorlike CB states are filled by electrons, building a fixed *net negative* charge at the interface which screens the applied positive gate bias or, to say it differently, repels

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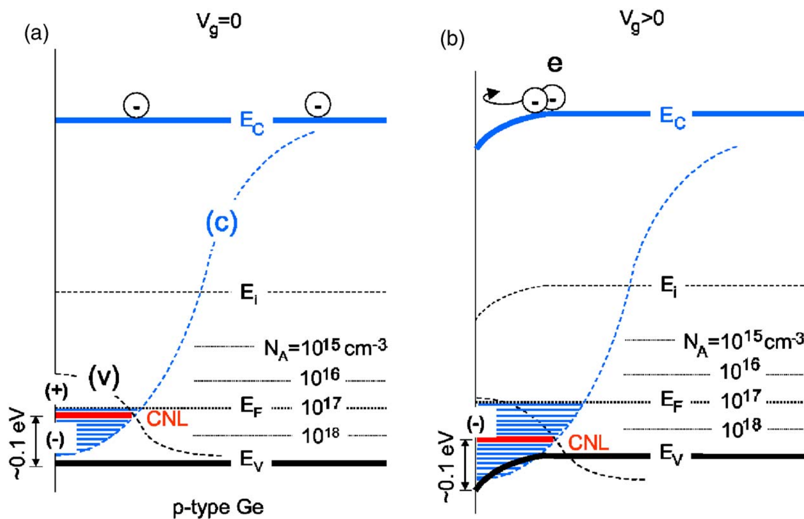

FIG. 3. (Color online) Energy band diagram drawn in scale for *p*-type Ge MOS structure (a) for zero gate bias V_g and (b) for a positive value of V_g. Here, only the semiconductor and the interface with the oxide insulator are shown. Dashed lines marked by (c) and (v) are arbitrary schematic representations of acceptorlike CB and donorlike VB densities of interface states, respectively. E_i is the midgap level. The horizontal dotted lines mark the position of the Fermi level for different doping concentrations.

mobile minority carriers (electrons) away from the surface. This makes it difficult to build an inversion layer, which in turn could severely affect operation of *n*MOSFET devices. This situation can be described effectively as the pinning of the Fermi level to retain charge neutrality at the interface. The problem could become more severe for lightly doped *p*-type Ge (see Fig. 3) since, in these cases, E_F is substantially higher than CNL, therefore more acceptorlike states could be filled. Note, however, that this predicts a different behavior compared to what is concluded in Ref. 11 In *n*-type Ge where E_F is located in the upper half of the band gap, an even larger negative charge could be trapped at the interface however, in this case, the built-up charge, attracting minority holes, helps invert the channel in *p*MOSFETs. In fact, the presence of negative fixed charge at the interface could shift the threshold voltage in *p*MOSFETs to positive values, resulting in a conducting channel at $V_g=0$ as previously observed.[5]

In summary, we have found that in metal/*n*-Ge Schottky diodes, the Fermi level is strongly pinned close to the CNL which is located only 0.09 eV above the VB. The location of CNL so close to the Ge VB could be the key to understand the asymmetry between *n*- and *p*-channel FET behaviors. In most of the cases of interest (in both *n*- and *p*-type Ge), the Fermi level in the semiconductor is above the CNL, resulting in a large buildup of fixed negative charge at the interface due to fillingup of acceptorlike states. Although this could be helpful in inverting the channel in *p*-FETs, on the opposite, the same built-up charge could prevent efficient inversion in *n*-FETs leading very often to nonfunctional or severely underperforming devices.

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