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Room-temperature single-electron charging phenomena in large-area nanocrystal memory obtained by low-energy ion beam synthesis

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We investigated the dependence of implantation dose on the charge storage characteristics of large-area *n*-channel metal–oxide–semiconductor field-effect transistors with 1-keV Si^+-implanted gate oxides. Gate bias and time-dependent source–drain current measurements are reported. Devices implanted with 1×10^{16} cm^{-2} Si dose exhibit a continuous (trap-like) charge storage process under both static and dynamic conditions. In contrast, for 2×10^{16} cm^{-2} implanted devices, electrons are stored in Si nanocrystals in discrete units at low gate voltages, as revealed by a periodic staircase plateau of the source–drain current with a low gate voltage sweep rate, and the step-like decrease of the time-dependent monitoring of the channel current. These observations of room-temperature single-electron storage effects support the pursuit of large-area devices operating on the basis of Coulomb blockade phenomena. © *2002 American Institute of Physics.*
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Single-transistor memory devices consisting of a metal–oxide–semiconductor (MOS) field-effect transistor (FET) with nanocrystals embedded in the gate oxide have recently attracted much attention as alternatives to conventional volatile and nonvolatile memories.[1,2] In addition, for the case of small (<10 nm) and uniform in size nanocrystals, quantum confinement and single-electron charging effects offer the possibility of quantized shifts of the transistor threshold voltage at room temperature.[3] The successful exploitation of these discrete changes may lead to the development of multilevel logic devices. This approach has been demonstrated in both nanoscale Si channel FET devices with a single (or few) nanocrystals[3–5] and in multiple dot memory devices (large-area FET) using Si nanocrystals formed by deposition on oxide–nitride tunnelling dielectrics.[6] However in the latter case, a fabrication route of forming high-density of small and uniform in size nanocrystals is an important issue to be resolved before the practical application of single-electron phenomena. For this reason, the *very-low energy* Si implantation technique is a promising candidate.[7] We recently explored the possibility of fabricating MOS memory devices through 1-keV Si^+ implantation of a thin thermal oxide (8 nm) and subsequent annealing.[8] Clear memory effects are observed for devices implanted with a dose of 1×10^{16} cm^{-2} or lower, while for higher implantation doses the lateral coupling of the Si nanocrystals at relatively high gate voltages is found to strongly affect the memory operation of the devices. In this letter, charge storage effects for the 1 (low dose) and 2 $\times10^{16}$ (high dose) cm^{-2} Si^+ fluences are investigated in the low gate bias regime. The step-like source–drain current versus time ($I_{DS}-t$) characteristics and the discrete threshold voltage shifts versus gate voltage (V_G), observed for the high dose implanted case, constitute evidence for room- temperature single-electron charging effects.

Memory devices with large channel width W and length L ($W/L=10/40$ μm) are fabricated in a manner similar to that used for conventional depleted-mode *n*-channel MOS transistors, except that the gate oxide bears silicon with a narrow distribution, peaking at a tunnelling distance from SiO_2/Si interface. For this purpose, Si is implanted at doses of 1×10^{16} or 2×10^{16} Si^+ cm^{-2} at 1 keV into 8 nm thick thermally grown SiO_2 film. Subsequently, a 30 nm thick SiO_2 layer is deposited, followed by a 30 min, 950 °C nitrogen annealing, aiming at the precipitation of Si nanocrystals. The nanocrystal characteristics (size, spatial distribution, and crystallinity) as a function of the implantation dose have been deduced earlier.[7] In brief: (a) The 1×10^{16} cm^{-2} dose gives rise to a Si-rich band with a thickness of about 3 nm located at 2–3 nm from the SiO_2/Si interface; the band is composed of low-density ill-crystallized quasi-spherical Si grains, 3–8 nm in size and (b) the 2×10^{16} cm^{-2} dose leads to the formation of a dense arrangement of crystallized platelet-like Si grains with a thickness about 4 nm and linear dimension ranging from 4–15 nm peaking at about 7–8 nm. Because of their dense arrangement, the nanocrystals appear as a quasi-continuous nanocrystalline layer located very close (1–2 nm) from the Si/SiO_2 interface. Electrical characterization of the resulting memory devices is performed at room-temperature under dark conditions.

The charge storage behavior of the implanted devices is investigated by monitoring the time evolution of the source–drain current for various gate voltages. Before each run, we hold V_G at -5 V for extended time to fully discharge the memory and then abruptly set the charging voltage. Figure 1 shows the room-temperature $I_{DS}-t$ curves for the low and high dose implanted devices and for 4.1 V gate voltage. Low-dose implanted devices exhibit a continuous source–drain current reduction indicating a continuous build up of negative charge in the insulator with time. This finding is attributed partly to the *low* density of Si grains formed and partly to the trap-like behavior of excess silicon atoms into

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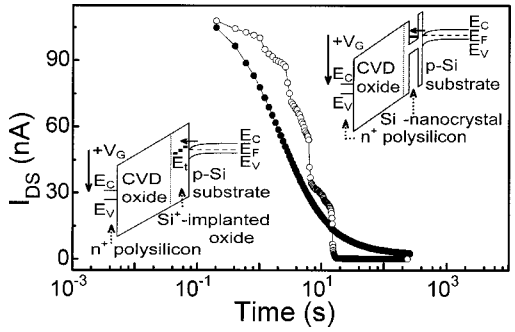

FIG. 1. Room-temperature I_{DS} vs time characteristics, for large-area channel MOSFETs with 1 (solid circles) and 2×10^{16} cm^{-2} Si^+ (open circles)-implanted gate oxides under 4.1 V gate voltage and 0.1V drain–source voltage (V_{DS}). Schematic energy band structures (insets) based on structural observation of the state of implanted silicon after annealing. Left-hand side inset: case of Si atoms distributed within the implanted oxide (1×10^{16} cm^{-2}); right-hand side inset: case of Si nanocrystal formation (2×10^{16} cm^{-2}).

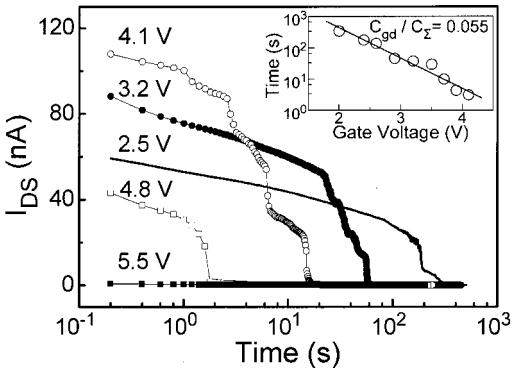

FIG. 2. Room-temperature $I_{DS}-t$ curves, for the case of a 2×10^{16} cm^{-2} Si^+-implanted device under different gate voltages and a 0.1 V drain–source voltage. Inset: time needed for the second injection event for different gate voltages. From the linear dependence, $C_{gd}/C_\Sigma=0.055$ is obtained.

SiO_2 matrix (Si atoms that do not form Si grains). Due to the low density of the Si grains, percolation transport through the low-resistive conduction paths in the channel causes a broadening of the quantized shifts in V_{Th}. In addition, it has been reported[9] that excess Si acts as a neutral trap with energy E_t at or above the Si conduction band. The tunneling probability is inversely proportional to the distance of the trap from the Si/SiO_2 interface. Thus, for the case of spatially distributed storage sites (low-dose case) and for constant V_G, the trap charging process continuously proceeds with time from traps closest to the SiO_2 interface to those further from the interface (left-hand side inset of Fig. 1), resulting in a continuous reduction of the source–drain current. In contrast, high-dose implanted devices show a step-like decrease of the source–drain current, a direct piece of evidence for a discrete charging mechanism. The formation of well-crystallized Si grains in dense arrangement is considered to be the origin of the observed current steps. Quantum confinement and Coulomb blockade effects inhibit the successive electron injection into the nanocrystals (right-hand side inset of Fig. 1), resulting in a discrete build up of charge in the insulator with V_G. The observed similar heights of the current steps indicate successive injection events of a single electron to each nanocrystal.

Figure 2 shows the $I_{DS}-t$ characteristics for the high-dose implanted device under various gate voltages. Clear injection events are observed for gate voltages lower than 4.3 V. The latter events occur at a low electric field (under 1 MV/cm) as a result of the lowered quality (due to excess silicon traps and implant-related damage) of the tunnel oxide.[8] For V_G higher than 5.5 V, the $I_{DS}-t$ curves do not exhibit any structure due to the fast charging response time. As we decrease the gate voltage, the position of the source–drain current steps shifts to longer times. The $I_{DS}-t$ curves are found to be reproducible during successive runs for the same V_G. The continuous reduction of the current, before the current steps appear, as well as the broadening of the steps are considered to originate from the background charge due to electron trapping within the defected tunnel oxide and/or within the few large nanocrystals with Coulomb gap lower than the room-temperature thermal energy (kT $\sim$26 meV). The continuous reduction of the current between the steps (instead of a flat plateau) is attributed to the large number of nanocrystals involved in the transistor channel screening. However, the similar heights of the current steps indicate that these nanocrystals have a narrow-size dispersion and located at about the same distance from the channel. It should be noted that for each gate voltage, the successive charge injection events are spaced at about equal distance in the logarithmic time scale. Based on the dynamic Coulomb blockade model proposed by Yano *et al.*,[3] we express the time (τ) needed for the next electron to come from the channel to the nanocrystal as: $\ln(\tau)=\text{const}-(e/kT)(C_{gd}/C_\Sigma)V_G$, where e is the electron charge, C_{gd} is the capacitance between the gate and the nanocrystal, and C_Σ is the total capacitance related to the nanocrystal. By plotting on a semilog plot the time needed for the second injection event for different gate voltages, a linear dependence is obtained (inset of Fig. 2). These findings constitute evidence for a single-electron charging effect.

In order to further investigate this possibility we estimate the capacitances for our structure. Neglecting the coupling between the nanocrystals and the source–drain extension regions (a reasonable assumption for a *large* channel area) and the coupling between adjacent nanocrystals (delocalization of electrons is expected at higher confinement energies[10] and thus at higher V_G) C_Σ is $C_{gd}+C_{cd}$, where, C_{cd}, is the capacitance between the channel and the nanocrystal. Based on our previous structural observations,[7] we approximate the nanocrystals as disk-shaped objects with a diameter of about 7.5 nm and a thickness (t_d) of 4 nm, and placed at a distance (t_{gd}) of 33 nm from the gate electrode and at a distance (t_{cd}) of 1–2 nm from the channel. In the plate capacitor approximation,[1] a value of 0.045 aF is estimated for the C_{gd}. The capacitance between the channel and the nanocrystal, $C_{cd,}$ depends strongly on the distance t_{cd}. From the experimental (inset of Fig. 2) value $C_{gd}/C_\Sigma=0.055$, we obtain $C_{cd}=0.770$ aF that corresponds[1] to $t_{cd}=1.3$ nm, a value in very good agreement with findings from direct structural observation.[7] The Coulomb energy E_C is given by $E_C=e^2/2C_\Sigma+E_n$. The first term is the classical electrostatic charging energy and is calculated to be 98 meV. The second term, due to quantum confinement, is the energy separation between the lowest subband and the second band and is estimated[10] to be 70 meV Since E_C is 168 meV, a value in

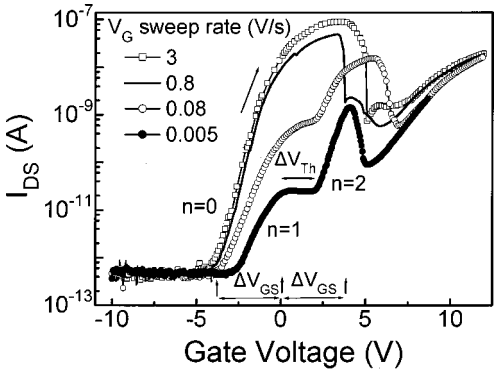

FIG. 3. Room-temperature transfer characteristics, for the case of 2×10^{16} cm^{-2} Si^+-implanted devices measured under different V_G sweep rates and $V_{DS}=0.1$ V. With decreasing sweep rate, the $I_{DS}-V_G$ curves show a clear staircase structure. The arrows indicate voltage regions ΔV_{GS} with 1 and 2 stored electrons per nanocrystal ($n=1$, 2), while the initial part of the fast swept $I_{DS}-V_G$ curve corresponds to $n=0$. ΔV_{Th} is the threshold voltage shift caused by the storage of a single electron per nanocrystal.

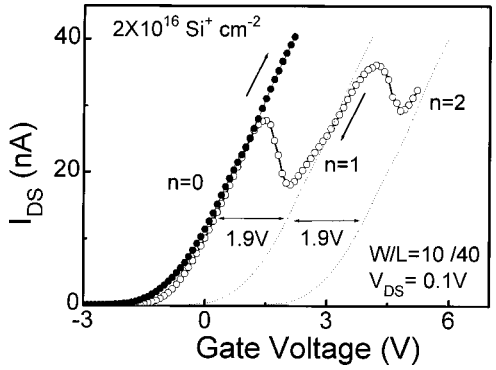

FIG. 4. Room-temperature I_{DS} current as V_G is swept forward (solid-circle curve) and backward after discharging (open-circle curve) at a rate of 0.8 V/s. The dot lines show $I_{DS}-V_G$ curves with $n=1$ and $n=2$ stored electrons per nanocrystal and are obtained by shifting the forward swept curve ($n=0$ stored electrons per nanocrystal) by 1.9 V and 3.8 V, respectively.

excess of 6 kT (for $T=300$ K), Coulomb blockade effect can be observed at room temperature.

The other evidence revealing a single-electron charging effect is the plateau structure of the I_{DS} versus V_G characteristics, shown in Fig. 3 for the high-dose case and measured under different V_G sweep rates. Electron injection in the nanocrystals during each measurement causes a dynamic shift of the threshold voltage V_{Th} of the device, resulting in the observed source–drain current structures. The time needed for an electron to come into the nanocrystal, strongly depends on V_G. Thus, for the case of a fast sweep, charge injection takes place at relative high V_G resulting in an efficient reduction of the I_{DS} due to the large number of injected electrons. The initial part of the $I_{DS}-V_G$ curve in this case corresponds to the uncharged state of the nanocrystals (number of electrons n in the nanocrystals equals zero, $n=0$). With decreasing sweep rate, V_G for electron injection decreases together with the number of involved electrons, resulting in the appearance of a plateau in the $I_{DS}-V_G$ curves. For a sweep rate slower than 5 mV/s (10 mV step and 2 s delay time), I_{DS} shows the same plateau indicating a self-limiting charging process. We argue that the $I_{DS}-V_G$ plateau structure is caused by the Coulomb blockade effect. In support of this claim is the periodicity of the plateau with period $\Delta V_{GS}=3.8$ V, shown in Fig. 3. The gate voltage increment ΔV_{GS} required for the addition of one electron into the nanocrystal ($\Delta V_{GS}=e/C_{gd}$) is calculated to be 3.6 V, a value that is very close to the experimental one. The ΔV_{Th} for one electron per nanocrystal is:[1] $\Delta V_{Th}=eAN_d/C_{gd}$, where N_d is the density of the nanocrystals and A is the effective capacitor area between the nanocrystal and the gate electrode. Putting the experimental ΔV_{Th} of 2V into this expression, we get $N_d=4\times10^{12}$ cm^{-2}, a value in agreement with electron microscopy data.[7] Such a high nanocrystal areal density reduces the low-resistance percolation paths in the channel and allows for the observation of the Coulomb blockade effect. However, the lateral coupling of the Si nanocrystals restricts the observation at the low V_G regime.

The quantized nature of electron removal from the nanocrystals is shown in Fig. 4. The $I_{DS}-V_G$ curves are obtained by sweeping V_G at a rate of 0.8 V/s. The solid-circle curve corresponds to the initial part of the forward sweep shown in Fig. 3, while the open-circle curve is obtained by backward sweeping, after discharging at $V_G=-5$ V. The observed sharp steps during the backward sweep suggest a discrete charge ejection process, while the magnitude of ΔV_{Th} is comparable to that obtained by the slow (5 mV/s) forward sweep shown in Fig. 3. The successive ejection of a single electron from each nanocrystal is inferred.

We have investigated the influence of implantation dose on the charge injection and storage mechanisms in large area MOSFETs structures with low energy Si^+-implanted and annealed gate oxides. Devices implanted at 1×10^{16} cm^{-2} exhibit a continuous charge injection and storage process due to the trap-like behavior of excess Si atoms in the SiO_2 matrix. In contrast, 2×10^{16} cm^{-2} implanted devices exhibit clear, step-like $I_{DS}-t$ and periodic staircase plateau $I_{DS}-V_G$ characteristics, both in support of the notion of room-temperature single-electron storage. The simple fabrication technique makes the *very-low energy* Si nanocrystal memory device an attractive option for low cost very large scale integrated memory and logic applications.

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