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Charge storage and interface states effects in Si-nanocrystal memory obtained using low-energy Si$^+$ implantation and annealing

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Thin SiO_2 oxides implanted by very-low-energy (1 keV) Si ions and subsequently annealed are explored with regards to their potential as active elements of memory devices. Charge storage effects as a function of Si fluence are investigated through capacitance and channel current measurements. Capacitance–voltage and source–drain current versus gate voltage characteristics of devices implanted with a dose of $1 \times 10^{16}\,cm^{-2}$ or lower exhibit clear hysteresis characteristics at low electric field. The observed fluence dependence of the device electrical properties is interpreted in terms of the implanted oxide structure. © *2000 American Institute of Physics.*
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In order to overcome limitations of conventional nonvolatile and dynamic memory devices, it has recently been proposed[1–3] to use nanocrystals as charge storage elements embedded in the gate oxide of a field-effect transistor and located in close proximity (2–3 nm) to the transistor channel. Floating gates consisting of Si or Ge nanocrystals have been fabricated through the use of various deposition techniques,[1,2] ion implantation and annealing,[2] or following[3] thermal oxidation of $Si_{1-x}Ge_x$. The ion implantation technique is attractive because of its well-established manufacturing advantages but faces the major challenge of making nanocrystals close to the channel without compromising the integrity of the gate oxide and the quality of the SiO_2/Si interface. For this purpose, *low*-energy Si implantation is a promising approach. Because of decreasing ion strangle with implantation energy, energies as low as 1 keV are suitable for making well-located two-dimensional (2D) arrays of Si nanocrystals at a relatively low dose and at a tunneling distance from the SiO_2/Si interface.[4] In order to explore the potential of this approach for memory applications, metal–oxide–semiconductor (MOS) capacitors and nMOS transistors with 1 keV Si implanted gate oxides are investigated.

Capacitors with $6.4 \times 10^{-4}\,cm^{-2}$ gate area and transistors with a gate length ranging from 2 to 10 μm and 100 μm gate width have been fabricated following a process similar to that used for conventional MOS devices. The main new element is the introduction of Si with a narrow distribution, peaking at a tunneling distance from the SiO_2/Si interface. For this purpose, Si implantation is carried out into 8-nm-thick thermally grown oxide at an energy of 1 keV and at doses ranging from 5×10^{15} to $5 \times 10^{16}\,cm^{-2}$. Subsequently, a 30-nm-thick control oxide is deposited, followed by a 30

min nitrogen annealing at 950 °C, aiming at the precipitation of Si nanocrystals. To investigate the effects of interface traps and defects originating from the nanocrystal fabrication process, aluminum sintering was carried out in N_2 and N_2/H_2 environment. The devices were characterized through bias and frequency dependent capacitance measurements, as well as static and dynamic transistor current measurements.

The nanocrystal characteristics as a function of the implantation dose were deduced from a transmission electron microscopy study combining cross-sectional and associated plane-view images and e-diffraction patterns. The major results are as follows: (a) The $5 \times 10^{15}\,cm^{-2}$ dose leads to very small ill-defined Si clusters. (b) The $1 \times 10^{16}\,cm^{-2}$ dose gives rise to a Si-rich band with a thickness of about 3 nm located at 2–3 nm from the SiO_2/Si interface; the band is composed of ill-crystallized quasispherical Si grains, 3–8 nm in size. (c) A $2 \times 10^{16}\,cm^{-2}$ dose or higher leads to well-crystallized plateletlike Si grains (4–15 and 5–20 nm in size for the 2 and $5 \times 10^{16}\,cm^{-2}$ cases, respectively) with a thickness $\sim$4 nm. These large Si nanocrystals are almost in touch with each other [Fig. 1(b) and plane-view images (not shown here) for the full (111) diffraction ring].

Figure 2 shows high-frequency (HF) capacitance–voltage (C–V) curves for nonimplanted and Si-implanted SiO_2 gate capacitors under dark conditions swept from -10 to $+10$ V and back to -10 V with a voltage step of 0.1 V/s. A clear hysteresis is found for the 5×10^{15} and $1 \times 10^{16}\,cm^{-2}$ cases and it corresponds to a flatband voltage shift (ΔV_{FB}) of about 4.6 and 10.0 V, respectively. The hysteresis is attributable to the trapping of electron/holes in the insulator during the positive/negative gate voltage sweep. Nonimplanted devices do not exhibit any shift in the C–V curves, showing that the hysteresis is Si implantation related. Furthermore, the observation of a large ΔV_{FB} at a low-

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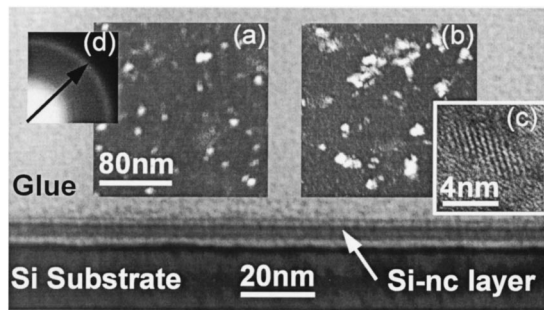

FIG. 1. Plane-view (PV) TEM micrographs from samples with a 8-nm-thick SiO$_2$ layer implanted with 2×10^{16} (a) and 5×10^{16} (b) Si$^+$ cm^{-2} at 1 keV and annealed at 950 °C for 30 min. Nanocrystals appear as open entities in (a) and (b). The cross-section image pertains to the (a) case. A high-resolution PV TEM image of a Si nanocrystal is shown in (c). The e-diffraction pattern (d) pertains to (a) (arrow indicates the {111} Si ring).

FIG. 3. Frequency dependence of the capacitance under accumulation conditions for three implantation doses and a reference. Fittings are for the 2 $\times10^{16}$ cm^{-2} (dashed line) and 5×10^{16} cm^{-2} (solid line) cases with indicated τ values, on the basis of the shown equivalent circuit.

electric field (<2.5 MV/cm) suggests that charge injection involves direct tunneling. From the above-mentioned findings we conclude that devices implanted with a dose of 1 $\times10^{16}$ cm^{-2} or lower exhibit the function of a memory. One memory state corresponds to excess electrons in the gate oxide and another to excess holes. In contrast, devices implanted with a dose of 2×10^{16} cm^{-2} or higher do not exhibit any memory effect. In this case the HF-C–V curves are significantly stretched out and the capacitance in the accumulation regime increases with the gate bias. For a better understanding of the HF-C–V results, the frequency dependence of the capacitance under accumulation is investigated (Fig. 3). A constant capacitance (~60 pF) is found for the nonimplanted, and the 5×10^{15} and 1×10^{16} Si cm^{-2} implanted devices. The observed capacitance corresponds to an effective SiO$_2$ thickness of about 37 nm, a value in agreement with the total oxide thickness of 37 ± 1 nm, determined by transmission electron microscopy (TEM) analysis. For the 2 and 5×10^{16} Si cm^{-2} implanted devices, the capacitance shows a strong frequency dependence. At low frequencies the capacitance saturates at about 75 pF, a value corresponding to an effective thickness of 29.5 nm (comparable to the 30 ± 1 nm TEM observed thickness for the deposited oxide). As the frequency increases, the capacitance becomes lower and asymptotically saturates at values corresponding to an effective thickness close to that for the nonimplanted device. These observations indicate that holes move between the Si-
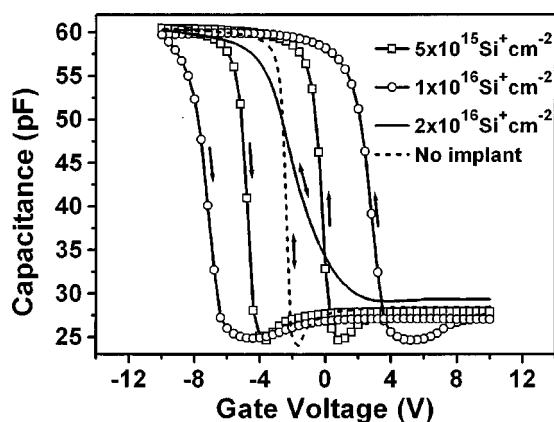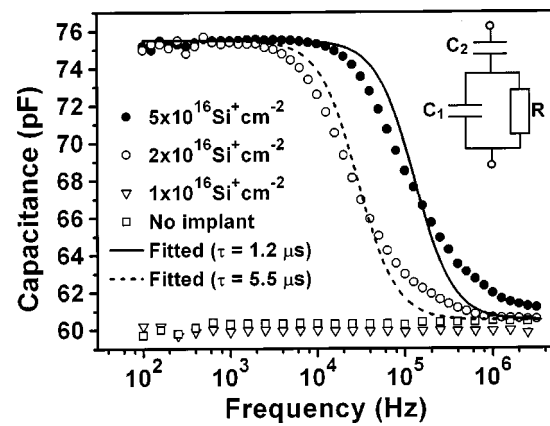

FIG. 2. High-frequency C–V characteristics for a reference (nonimplanted) and Si-implanted SiO$_2$ gate capacitors at three different doses.

nanocrystal layer and the Si substrate in phase with the small amplitude modulation (25 mV$_{p-p}$). The characteristic time constant, τ, for this dynamic hole exchange can be obtained[5] by considering τ as the only parameter to fit the experimental results to the theoretical capacitance derived from the equivalent circuit shown in the inset of Fig. 3. C_1 is the Si-nanocrystal/SiO$_2$/Si-substrate junction capacitance, C_2 is the Si-nanocrystal/deposited oxide/n^+-poly-Si gate junction capacitance, and R is the tunneling resistance of the first junction (the resistance of the deposited oxide is considered as infinite). R is inversely proportional to the transition rate between a Si nanocrystal and the substrate, and is strongly affected by the thickness and quality of the injection oxide, as well as by the size of the nanocrystals. Fitted results for the 2 and 5×10^{16}Si cm^{-2} implanted devices indicate characteristic times of 5.5 and 1.2 μs, respectively, for a gate voltage of -10 V. More negative gate bias leads to shorter characteristic times, while longer times are observed for a lower negative bias. This is because the coupling between the accumulation layer and the Si nanocrystals depends on the charge density in the nanocrystals. The charge density is governed by the transition rate between the substrate and the nanocrystals, and is affected by the lateral coupling between the nanocrystals.

For the 2 and 5×10^{16} Si cm^{-2} implanted devices, where the nanocrystals appear to be coupled laterally (i.e., the layer of nanocrystals is quasicontinuous), charge injection through the more conductive paths in the defective oxide leads to a strong charging of the nanocrystals. As the defect states in the oxide introduced by ion implantation and also the extent of the lateral coupling between the nanocrystals are both expected to vary with dose, a lower dose gives rise to a longer characteristic time, in agreement with our observations for the 2 and 5×10^{16} cm^{-2} cases. The very long characteristic times observed for low implantation doses ($<2\times10^{16}$ cm^{-2}) are due to the improved quality of the oxide and the structural arrangement of the Si material after annealing. The traplike behavior of excess Si[6] expected in the case of 5×10^{16} cm^{-2} and/or the presence of electronic states at the surface of the uncoupled Si grains (case of 1 $\times10^{16}$ cm^{-2}) lead to an increased charge storage time in the oxide and cause the flatband voltage shifts shown in Fig. 2.
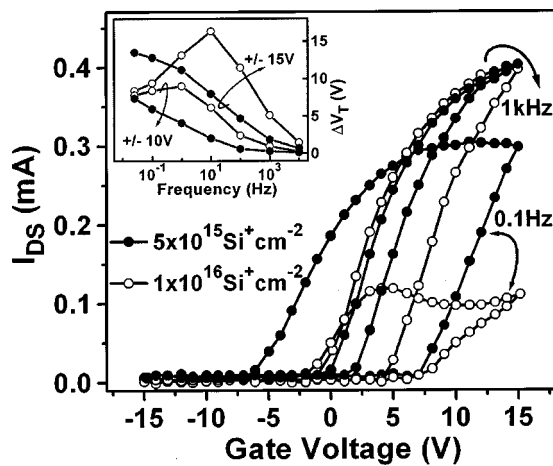
FIG. 4. Source–drain current vs gate voltage (triangular signal) of nMOS transistors with a 4 μm gate length for two Si implantation doses and two different sweep rates (frequencies). The device threshold voltage shift (ΔV_T) vs frequency of $+15/-15$ V and $+10/-10$ V V_G triangular signals is shown in the inset. The drain voltage was fixed at 0.1 V.

FIG. 5. Logarithmic and linear (inset) transfer characteristics for 1 $\times 10^{16}$ Si cm^{-2} implanted, H$_2$- and N$_2$-annealed devices. The gate voltage is swept continuously from -15 to $+15$ V.

The transfer characteristics of nMOS transistors with 5×10^{15} cm^{-2} and 1×10^{16} Si cm^{-2} implanted gate oxides under different gate voltage sweep rates appear in Fig. 4. The measurements were performed in a way similar to that of Ohzone *et al.*[7] A load resistor ($R_L = 100 \, \Omega$) is connected between the source electrode and ground to monitor the source–drain current I_{DS} through source voltage ($V_s = I_{DS}R_L$) measurements. Triangular signals of $+15/-15$ V and $+10/-10$ V amplitude (V_G) were applied to the gate electrode for a wide range of frequencies. A strong reduction of the source–drain current is observed, as the frequency of the V_G signal decreases. The magnitude of the source–drain current suppression is found to depend on the implantation dose. This effect can be related to the interface traps generated by ion implantation. It has been reported that excess Si at the Si/SiO$_2$ interface acts as a slow interface trap in thermal equilibrium with the Si substrate. The occupancy of these traps in the inversion regime results in the accumulation of negative charge close to the Si/SiO$_2$ interface. This charge accumulation effect reduces the mobile charge density in the transistor channel. Figure 4 (inset) shows the dependence of the threshold voltage shift (ΔV_T) on the gate voltage sweep rate. For 5×10^{15} Si cm^{-2} implanted devices, ΔV_T monotonically increases as the frequency decreases, with a tendency for saturation in the $+15$ V/-15 V V_G regime. In the case of 1×10^{16} Si cm^{-2} implanted devices and for a $+15$ V/-15 V V_G signal, ΔV_T increases continuously up to 10 Hz and then decreases significantly, approaching saturation values lower than that for the 5×10^{15} cm^{-2} case. For a V_G signal of $+10$ V/-10 V, ΔV_T increases up to 1 Hz and then slightly decreases, reaching saturation values similar to those measured in the $+15$ V/-15 V V_G regime. The decrease of the threshold voltage shift observed for the 1×10^{16} cm^{-2} case in the low frequency regime can be attributed to a dynamic charge exchange between the nanocrystals and the transistor channel during the measurement. Because a nanocrystal has a larger capture cross section than the defects related to the implantation (case of 5×10^{15} cm^{-2}) or those located at the nanocrystal–oxide
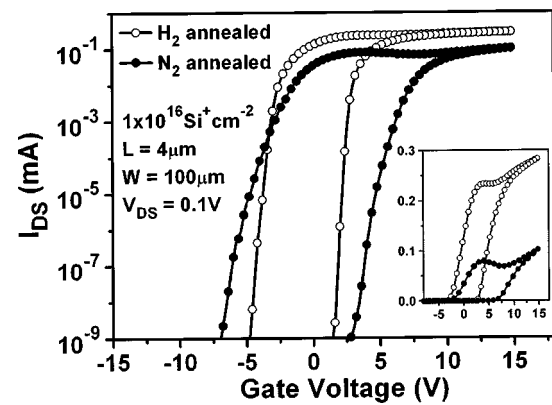
interface (case of 1×10^{16} cm^{-2}), the observed dynamic charge exchange mainly takes place through the nanocrystal electronic states and the inversion layer. This implies a thermal activation process as an electron injected into a nanocrystal is localized at an interface defect. The suggested mechanism is supported by our experimental results at low temperature (77 K), where the threshold voltage shift increases monotonically as the frequency decreases.

Figure 5 shows the effect of H$_2$ annealing treatment on the logarithmic and linear (inset of Fig. 5) transfer characteristics of a 1×10^{16} Si cm^{-2} implanted device. $I_{DS} - V_G$ characteristics are substantially improved after H$_2$ treatment, resulting in a subthreshold swing (SS) of 0.32 V/decade and an ON-current (I_{ON}) of 250 μA, compared to a SS of 0.44 V/dec and I_{ON} of 80 μA for N$_2$-annealed devices. This observation suggests that hydrogen passivates silicon-dangling bonds at the Si/SiO$_2$ interface, thereby reducing the interface trap density. Moreover, the threshold voltage window is larger for the N$_2$-annealed devices, indicating that H passivation also takes place at the Si–nanocrystal/SiO$_2$ interface.

In brief, we have explored the possibility of fabricating MOS memory devices through very-low-energy (1 keV) Si$^+$ implantation. Device electrical characteristics correlate strongly with the spatial arrangement and structural state of implanted Si as well as with the presence of various defects/traps in the injection oxide and at the Si nanocrystal/SiO$_2$ and SiO$_2$/Si substrate interfaces. Clear memory characteristics are observed for doses less than 2×10^{16} cm^{-2} and low electric fields.

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