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Reliability Issues and Electrical Characteristics of Rare-earth oxides and their Gate Stacks grown on Germanium Substrates

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Ph.D. Dissertation

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Dedicated to my newborn baby, AARAF

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ΠΕΡΙΛΗΨΗ

Η παρούσα Διατριβή εξετάζει θέματα αξιοπιστίας και τα ηλεκτρικά χαρακτηριστικά Οξειδίων Σπάνιων Γαιών και αντίστοιχων στοιβών διηλεκτρικών, ανεπτυγμένων πάνω σε υποστρώματα Γερμανίου. Το Γερμάνιο, σε αντικατάσταση του Πυριτίου προσφέρει μεγαλύτερη ευκινησία ηλεκτρονίων (2x) και οπών (4x) στα αντίστοιχα κανάλια τρανζίστορ τύπου MOSFET. Μελλοντικά, η τεχνολογία MOS, με κανάλι Γερμανίου αναμένεται να εφαρμοσθεί σε πλατφόρμες Πυριτίου, λόγω της βελτιωμένης ταχύτητας φορέων. Τα κρίσιμα χαρακτηριστικά επίδοσης των (MOS) πυκνωτών και τρανζίστορ καθορίζονται από τη διεπαφή των υλικών high-κ και του Γερμανίου. Η φτωχή ποιότητα του ενδογενούς οξειδίου (GeO_2) παρεμπόδισε τη χρήση των υλικών αυτών σε παραγωγή μεγάλης κλίμακας. Τα Οξείδια Σπάνιων Γαιών (REOs) όπως τα CeO_2, La_2O_3, Dy_2O_3, Gd_2O_3 μπορούν να εναποτεθούν άμεσα σε υποστρώματα Γερμανίου. Αλληλεπιδορύν έντονα με το υπόστρωμα, παράγοντας αυθόρμητα (κατά την εναπόθεση) ένα διεπιφανειακό στρώμα το οποίο περιέχει οξειδωμένο Γερμάνιο με βελτιωμένα ηλεκτρικά χαρακτηριστικά. Τα χαρακτηριστικά αξιοπιστίας αυτών των MOS σε υπόστρωμα Γερμανίου έχουν ιδιαίτερη σημασία και αποτελούν το κύριο θέμα της παρούσας διατριβής .

Η παγίδευση φορτίων αποτελεί μείζονα παράγοντα αναφορικά με την αξιοπιστία στις περισσότερες αστάθειες των διατάξεων υλικών high-k. Κατά την υψηλού πεδίου έγχυση σήραγγας ηλεκτρονίων στο στρώμα του οξειδίου, δημιουργούνται στο σύστημα διηλεκτρικού/ημιαγωγού μικροσκοπικά ελαττώματα όπως οι φυσικές παγίδες ηλεκτρονίων, η παγίδευση φορτίου και οι καταστάσεις διεπαφής. Οι φυσικές παγίδες ηλεκτρονίων που δημιουργούνται κατά την καταπόνηση υψηλού πεδίου μπορούν να προκαλέσουν την έγχυση ηλεκτρονίων σε χαμηλές τάσεις, προκαλώντας ρεύμα διαρροής stress-induced leakage current (SILC). Η αυξημένη σημασία του ρεύματος διαρροής stress-induced leakage current (SILC) στα χαμηλής ισχύος ULSI και στις μη πτητικές εφαρμογές μνήμης έχει αναγνωρισθεί εδώ και καιρό. Το SILC περιγράφεται από μια διαδικασία σήραγγας υποβοηθούμενης από παγίδες

(TAT) μέσω των παγίδων οξειδίου που παράγονται από την καταπόνηση. Η πειραματική μέτρηση της ενεργειακής κατανομής των παγίδων αποτελεί κύριο μέλημα προκειμένου να κατανοηθεί ποσοτικά η διαδικασία SILC. Παρά το γεγονός ότι το transient SILC ρεύμα παρέχει χρήσιμες πληροφορίες για την κατανομή των παγίδων οξειδίου, απουσιάζει μια προσεκτική ανάλυση της μεταβατικής διαδικασίας, λαμβάνοντας υπόψη και φαινόμενα σήραγγας ηλεκτρονίων και οπών. Άλλο ένα σημαντικό στοιχείο αποτελούν οι αστάθειες λόγω της συγκέντρωσης φορτίων στη διεπαφή των δυο διηλεκτρικών. Πράγματι, το gate stack bilayer προκαλεί παγίδευση φορτίων, ενώ ορισμένες φορές επιδεικνύει και διηλεκτρική χαλάρωση και το συνδυασμένο αυτό φαινόμενο ονομάζεται Maxwell-Wagner - Instabilities.

Στο κεφάλαιο 3 ερευνήθηκαν οι επιπτώσεις της παγίδευσης φορέων, του SILC και των συνοριακών παγίδων στο CeO_2, εφαρμόζοντας τη μέθοδο "stress and sense". Παρατηρήσαμε ότι τα χαρακτηριστικά παγίδευσης φορτίου και το SILC εμφανίζουν συμπεριφορά εξαρτώμενη από το δυναμικό. Δείξαμε επίσης ότι η παγίδευση φορτίου αποτελεί τον υπερισχύοντα μηχανισμό κατά την καταπόνηση χαμηλού πεδίου ενώ σε υψηλότερα πεδία το SILC επικρατεί έναντι των χαρακτηριστικών της παγίδευσης φορτίων. Η παγίδευση φορτίων και το SILC μαζί μπορούν να εξηγηθούν από το μοντέλο του Nigam, το οποίο αρχικά αναπτύχθηκε για το Si/SiO_2. Επίσης αναπτύσσουμε ένα μοντέλο για να εξηγηθούν τα χαρακτηριστικά παγίδευσης φορέων σε διαφορετικής έντασης πεδία καταπόνησης. Στο κεφάλαιο 4 περιγράφονται οι μηχανισμοί μεταφοράς ρεύματος στο CeO_2 και παρουσιάζεται πως στα χαμηλά πεδία επικρατεί η εκπομπή Schottky ενώ στα υψηλότερα η μετάδοση Poole-Frenkel.

Στα κεφάλαια 5-6, το Stress-induced leakage current (SILC), η παγίδευση φορέων και η διηλεκτρική χαλάρωση εξετάζονται σε Πύλες στοίβας HfO_2/Dy_2O_2. Σε χαμηλά πεδία, το φαινόμενο SILC είναι αμελητέο αλλά σε μεγαλύτερα πεδία ακολουθεί ένα νόμο δύναμης. Σχετικό εύρημα αποτελεί και η αστάθεια Maxwell-Wagner. Το gate stack επέδειξε αρχικά διηλεκτρική χαλάρωση και ακολούθησε παγίδευση φορέων καταλήγοντας σε διηλεκτρική κατάρρευση. Πράγματι, η Πύλη στοίβας είναι η αιτία της παγίδευσης φορτίων.

ABSTRACT

Germanium as a replacement for Silicon in metal-oxide-semiconductor (MOS) devices, offers a higher electron (2x) and hole (4x) mobility than silicon. A Ge channel MOS technology has been expected to be implemented into future high-speed Si platform, because of the enhanced carrier transport. The critical performance characteristics of (MOS) capacitors and transistors are determined by the interface between the high-κ materials and Ge. The poor quality of the native oxide (GeO_2) however hampered the use of this material in large scale production. One potential solution is the use of Rare-earth oxides (REOs) such as CeO_2, La_2O_3, Dy_2O_3, Gd_2O_3, which can be directly deposited on Germanium substrates. They form strongly interacting interfaces, producing spontaneously (during deposition) an interfacial layer which contains oxidized Ge with improved electrical characteristics. The reliability characteristics of these MOS devices on Germanium substrates are of important concerns and the main subject of the present work.

Charge trapping is a major reliability concern in most of the high-k material devices. During high field injection of electrons into the oxide layer, microscopic defects like neutral electron traps, and interface states are generated in the dielectric/semiconductor system. The neutral electron traps generated during high field stress can act as a stepping stone for the injected electron at a low voltage, giving rise to a stress-induced leakage current (SILC). The increased importance of the stress-induced leakage current (SILC) in ULSI low-power and non-volatile memory applications has long been recognized. SILC has been described by a process of trap-assisted tunneling through stress generated oxide traps in Si/SiO_2 MOS devices. The experimental measurement of the trap energy distribution represents therefore a primary concern in order to quantitatively understand the SILC process. Although the transient SILC current has been shown to provide useful information about the oxide trap

distribution, a careful analysis of the transient processes, is still lacking. Another important issue is current instabilities due to charge accumulation at the interface of any two dielectrics, that is, gate stack bilayer itself causes charge trapping, sometimes also demonstrate dielectric relaxation, and these combined effects are termed Maxwell-Wagner - Instabilities.

The present work comprises of six (6) chapters, chapter # 1 dealing with the theoretical background and chapter # 2 with the Experimental part. In chapter # 3 the effects of charge trapping, SILC, and border traps in CeO_2 films grown on Ge substrates are investigated, where the subsequent analysis proves that charge trapping characteristics and SILC show voltage dependence behaviour. It is also shown that at low stress field charge trapping is the dominant mechanism while at higher stress field SILC prevails over charge trapping characteristics. Both mechanisms can be explained by a model, which was originally developed for the Si/SiO_2 system. We also develop a model to explain the charge trapping characteristics at different stress fields. In chapter # 4 the current conduction mechanisms in CeO_2 thin films are reported which are governed by Schottky emission at low fields that turn to Poole-Frenkel conduction at higher fields.

In chapter # 5-6 the Stress-induced leakage current (SILC), Charge trapping and Dielectric relaxation effects in HfO_2/Dy_2O_2 gate stacks are discussed. At low field the SILC effect is negligible while at higher fields it follows a power law. A pertinent finding from this system is that it shows Maxwell-Wagner instability. The MOS devices show initially dielectric relaxation effects followed by charge trapping that finally reaches dielectric breakdown. As a matter of fact, the gate stack itself is the cause of charge trapping.

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Chapter-1

Introduction

1.1 Introduction

It is well known that compared to Silicon (Si) the use of Germanium (Ge) would bring significant enhancements to low field carrier mobilities for both electrons and holes. Gains up to 2x for electrons and 4x for holes have been reported for bulk germanium [1-4]. Ge is also more compatible than Si with most of the high-κ materials that have been proposed for gate insulators. This is because, as opposed to the case of silicon, there is no stable phase of germanium oxide that would form incidentally an additional penalizing layer during the deposition of high-k oxides. One drawback of germanium is related to its smaller optical bandgap ($E_g \sim 0.67$eV), which raises concerns about junction leakage. For this reason in particular, it is expected that if germanium comes into mainstream CMOS, it will be in the form of GeOI films. This will provide all the benefits of silicon in terms of mechanical properties, weight, cleanliness, and flatness. Beyond CMOS channel mobility improvement that could allow extending Moore's law, Ge is also an enabling solution for combining different functions on the same substrate. Ge can be used directly as an active material for near-infrared photo-detectors.

The scaling of MOSFETs has been following the famous Moore's law, which is often stated as the doubling of transistor performance and quadrupling of the number of devices on a chip every three years [5]. This law is shown in Figure 1.1, where the number of MOS transistors integrated in the different generations of Intel's microprocessors is presented as a function of the production year [6].

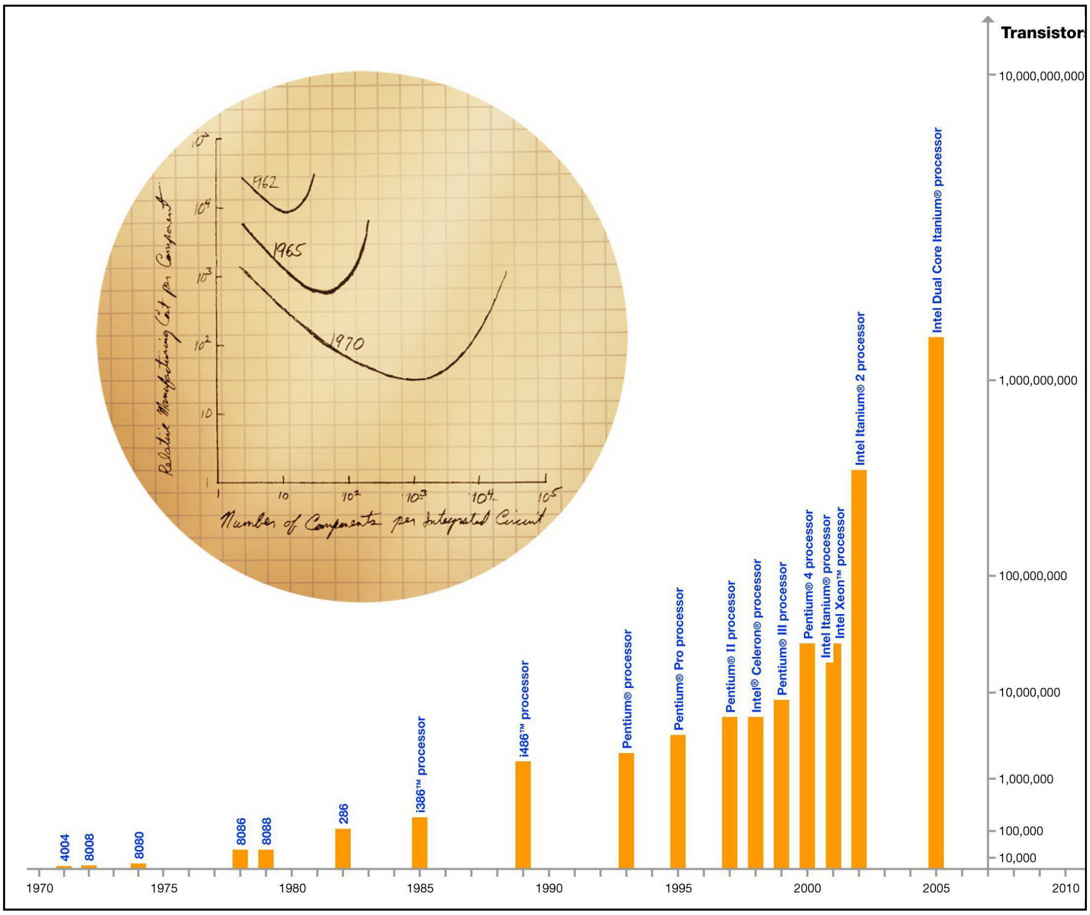

Figure 1.1: *Illustration of Moore's law: number of transistors integrated in the different generations of Intel's microprocessors vs. the production year. After Ref.[6].*

Next-generation Intel® Itanium® processors (codenamed Tukwila) take the next big leap in processor-based server technology. As the world's first 2-billion transistor microprocessor since January 2008, Tukwila is designed to provide highly scalable and reliable performance for mission-critical enterprise server solutions [7].

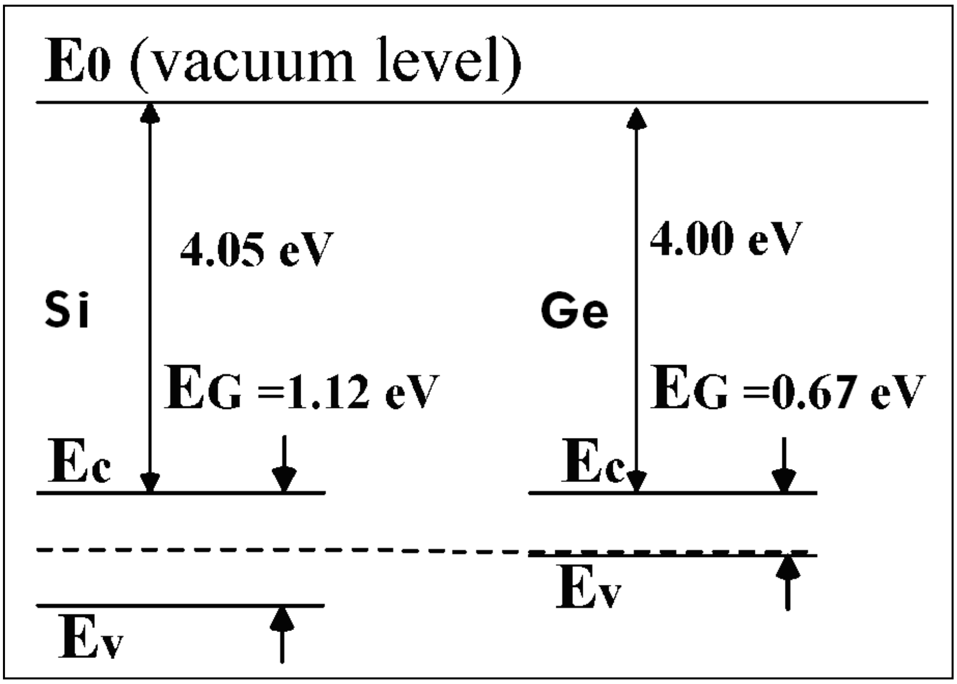

Figure 1.2: *Comparison between Si and Ge band-diagrams. The valence band edges differ by 0.51 eV. The dashed line shows the mid bandgap level of Si.*

As a group IV semiconductor, germanium (Ge) is expected to display many of the same properties as silicon (Si). Yet, despite its better bulk electrical performances (higher hole and low-field mobilities, and narrower bandgap) [8], Ge has not been used much in the past because its oxide is much less stable than SiO_2. As a result, the electrical properties of the Ge/GeO_x interface are much worse than for Si/SiO_2, where x is used to emphasize that GeO_2 is not necessarily the dominant oxide form for germanium. The nature of germanium oxide is such that wet chemical procedures for cleaning Ge (so critical for device fabrication) have been very challenging to establish. Yet, with renewed interest for high mobility substrates as Si is reaching some of its fundamental limits, the need to understand and control the passivation of Ge surfaces is even greater.

The success of Si CMOS technology for decades is partly due to the existence of stable oxide and high-quality SiO_2/Si interface, which is in direct contact with CMOS channel region and permits low defect charge density ($\sim 10^{10}$ cm^{-2}) and interface state density ($\sim 10^{10}$ $cm^{-2}eV^{-1}$), providing high performances of CMOSFET and reliability characteristics. In addition, the recent technological progress in high-κ gate dielectric has increased the possibility of high-κ/Ge system to be implemented for future gate stack. However, past decade studies on high-κ/Ge system indicate that tremendous efforts should be paid on the high-κ interface engineering in order to achieve successful scaling of Equivalent Oxide Thickness (EOT) with low-leakage current, good sub-threshold characteristics, high carrier mobility, and acceptable reliability.

Continued scaling of device dimensions has led to greater emphasis on such issues, and indeed fundamental limits imposed by gate leakage and intrinsic reliability are expected to prevent reduction of the thickness of the high-κ gate dielectric in MOS. As a matter of fact, reliability issues, like, charge trapping, stress-induced leakage current (SILC), oxide degradation, dielectric relaxation (DR), as well as, Maxwell-Wagner instability because of bilayer high-κ gate stacks itself, are important reliability concerns. Charge trapping causes the threshold voltage to shift with stressing time and is therefore an important transistor reliability issue. SILC is now the limiting factor for down scaling the tunnel oxide thickness in floating-gate based non-volatile memories. A potentially serious device integration problem exists with metal-oxide high-k dielectrics such as HiO_2 and ZrO_2. Due to DR, the problem is that an applied voltage causes these materials to develop a residual polarization that can remain long after the voltage is removed [9].

1.2 High mobility Germanium: possibly a future material for Microelectronics

In 1947, the first transistors were fabricated in Bell Labs using bulk germanium as the semiconducting material. For this work its inventors, John Bardeen and Walter Brattain shared the 1956 Nobel Prize in Physics, along with William Shockley. However, by the 1960s its use was largely supplanted with Si due largely to Si's high quality thermal oxide. About a dozen years later, the integrated circuit was independently invented by Jack Kilby, who used Ge substrates, and by Robert Noyce, who used silicon, and for which Kilby received the 2000 Nobel Prize in Physics (Noyce had passed on in 1990). Today, with the 45 nm technology node in production, high-κ dielectrics are beginning to replace SiO_2 in the gate, and as such, one of the key reasons for using Si is no longer as relevant. This, combined with performance concerns for Si based devices for and beyond the 22 nm node has made Ge a worthy area for research for high performance devices [10].

In the years since the turn of the millennium, there has been significant progress towards the replacement of the SiO_2 gate dielectric with high dielectric constant (high-κ) materials like HfO_2 and HfSiO(N). With feasible replacements for SiO_2, the key drawback of Ge, namely the lack of a high quality native oxide, becomes much less significant. This progress in high k R&D, plus the better electron (3900 vs 1400 cm^2/Vs) and hole (1900 vs 500 cm^2/Vs) mobilities for Ge over Si has led to a resurgence of interest in Ge [10].

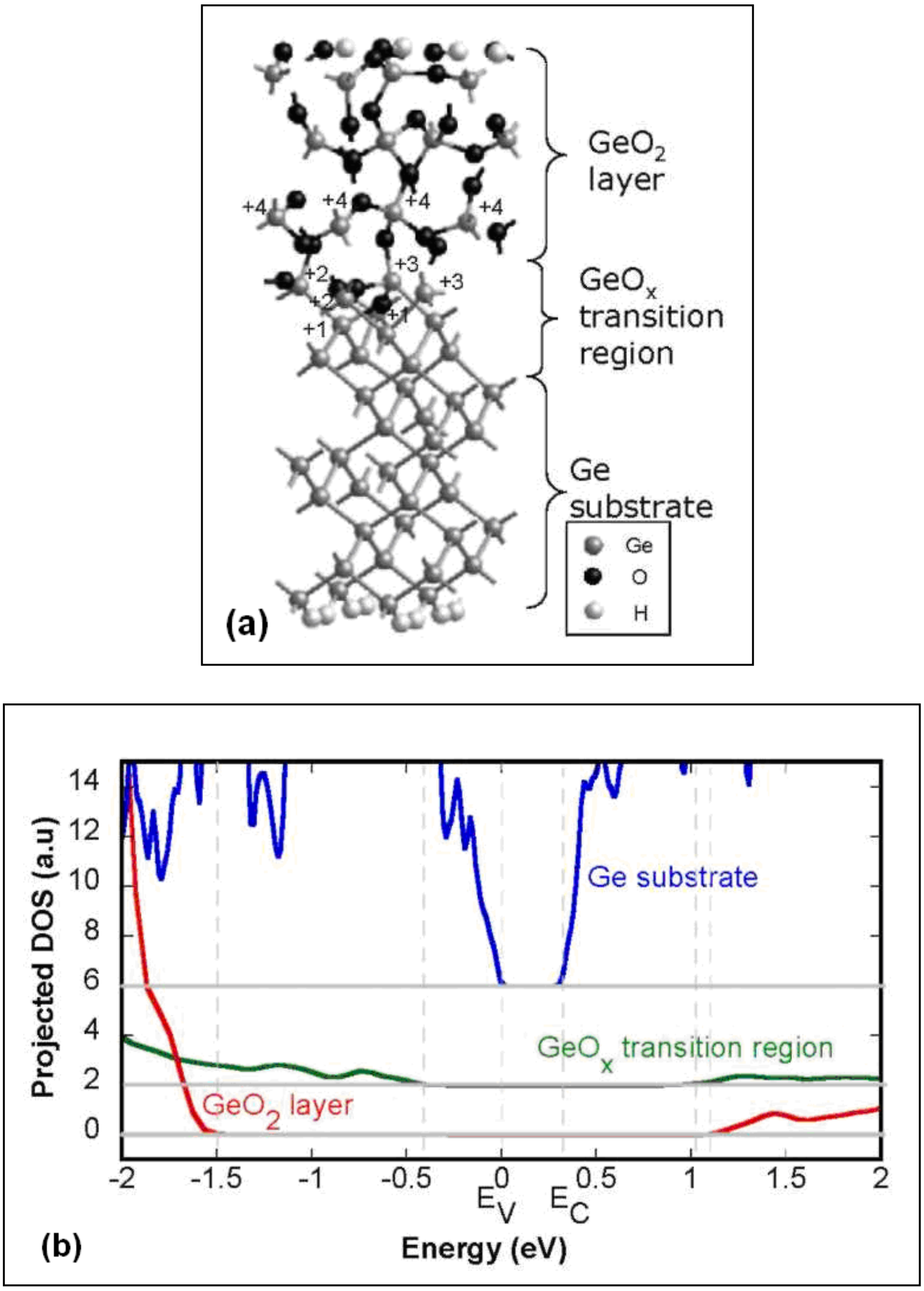

Fig. 1.3: *(a) Simulated cell for oxidation of Ge to GeO_2 (Ge 4+ oxidation state), with a GeOx transition region comprised of Ge in the 1+, 2+ and 3+ oxidation states. (b) Projected Density of States (DOS) for the Ge substrate, GeO_x transition region, and GeO_2 layer, showing that neither GeO_2 nor GeO_x states fall within the Ge bandgap. After Ref. [11]*

Germanium devices obviously require a substrate for fabrication. The development of effective germanium passivations and gate dielectrics poses a major challenge for germanium

MOS. Density functional theory simulations of a germanium sub-oxide transition region between a Ge substrate and a GeO_2 layer show no states in the Ge bandgap for either the GeOx transition region or the GeO_2 layer, as indicated in Fig. 1.3 (a) and (b). These simulated results suggest that there may be no inherent reason for poor electrical behavior for germanium oxide; rather the poor behavior typically seen could be due to extrinsic effects. For Ge, 2+ and 4+ are the only common oxidation states and GeO and GeO_2 are the only observed bulk oxides [12].

1.3 High κ gate dielectrics

1.3.1 Introduction

The dielectric constant (κ) is a measure of a material's ability to resist the formation of an electrical field within it. Low dielectric constant materials, such as air, show almost no change in orientation of molecules when a voltage is applied. Materials with high dielectric constants polarize their structures to counteract fields they experience. One can model the bonds in these structures as dipoles. As the strength of these dipoles increases, a stronger alignment of the dipoles will be resulted, which often leads to an increased κ value. These aligned dipoles also produce an image charge effect at the dielectric/doped silicon layer interface.

1.3.2 Limitation of SiO_2

The main problem arising from the scaling of the SiO_2 layer thickness concerns the leakage current flowing through the metal-oxide-semiconductor structure. As a matter of fact, in ultrathin SiO_2 gate layers (thickness typically below 3nm) the charge carriers can flow through the gate dielectrics by a quantum mechanical tunneling mechanisms [13-14]. Another issue related to the thickness scaling concern reliability aspects. During the operation of the MOSFETs in integrated circuit, charge carriers flow through the devices, resulting in the generation of defects in the SiO_2 gate layer and Si/SiO_2 interface [15-16]

When a critical density of defects is reached, breakdown (or quasi-breakdown) of the gate layer occurs, resulting in the failure of the devices [17-18]. It was shown by Degraeve *et al.* [19] that the time-to-breakdown distributions of the ultrathin SiO_2 layers could be quite well produced by a percolation approach, assuming that breakdown occurred via the formation of a percolation path between defects generated during the electrical stress.

The SiO_2 thickness limit at technological specifications (ITRS) is found to be about 2.2nm at room temperature, and 2.8nm at 150^0C. Reliability requirements thus appear even more severe than the leakage current requirements with respect to the scaling of the SiO_2 layer thickness [20].

1.3.3 Alternative High-κ dielectrics

From an electrical point of view, the metal oxide semiconductor structure behaves like a parallel plate capacitor: when a gate voltage V_g is applied to the gate, charges on the metal are compensated by opposite charges in the semiconductor, these latter charges forming the channel connecting the source and the drain of the transistor. The capacitance C_{OX} of this parallel plate capacitor is given by

$$C_{OX} = \frac{\kappa \varepsilon_0 A}{t_{OX}} \tag{1.1}$$

with κ being the dielectric constant (also referred to as permittivity) of the oxide, ε_0 being the permittivity of free space (8.85×10^{-14} F/cm), A being the capacitor area, and t_{OX} being the thickness of the oxide.

From equation (1.1) it appears that decreasing t_{ox} allows us to increase the capacitance of the structure to have low equivalent oxide thickness (EOT), and hence increase in the number of charges in the channel for a fixed value of V_g. However, as pointed out above, the SiO_2 layer thickness approaches its limits. An alternative way of increasing the capacitance is to use an insulator with a higher relative dielectric constant than SiO_2 (it should be noticed that the relative dielectric constant is also represented by the letter κ. and one speaks about high-κ materials). One could then use a thicker gate layer and, hopefully, reduce the leakage current flowing through the structure and also improve the reliability of the gate dielectric.

The equivalent oxide thickness (EOT) of a material is defined as the thickness of the SiO_2 layer that would be required to achieve the same capacitance density as the high-κ material in consideration. According to equation (1.1), is thus given by

$$\frac{EOT}{\varepsilon_{r,SiO_2}} = \frac{t_{high-\kappa}}{\varepsilon_{r,high-\kappa}}$$

$$EOT = \frac{\varepsilon_{r,SiO_2}}{\varepsilon_{r,high-\kappa}} t_{high-\kappa} \tag{1.2}$$

where $t_{high-\kappa}$ and $\varepsilon_{r,high-\kappa}$ are the thickness and relative dielectric constant of the high-κ material, respectively. As an example, using ZrO_2 as gate dielectric ($\kappa = 20$) would allow us to use a 5.1 nm thick layer in order to achieve a capacitance equivalent to a 1 nm thick SiO_2 layer; the equivalent oxide thickness of this ZrO_2 layer is thus 1 nm.

Actually, when a high-κ metal oxide like ZrO_2 or HfO_2 is deposited on a Ge substrate, an ultrathin low-κ interfacial layer, either GeO_x or GeM_yO_x, (where M is Zr or Hf) forms at the Germanium interface, as illustrated in Fig. 1.4. This interfacial layer may

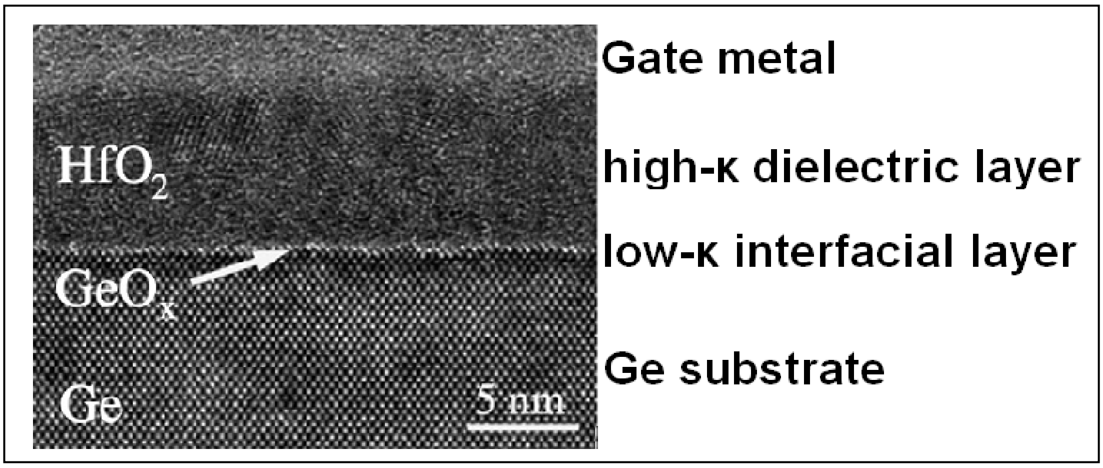

Fig. 1.4: *Schematic illustration of MOS structure with a high-κ gate stack, formed by a low – κ interfacial layer and a high-κ dielectric layer. After Ref. [21]*

grow either during the deposition of the high-κ dielectric or during post-deposition anneal processes. It should be noticed that another low-κ layer can also form at the high-κ dielectric/metal gate interface.

The capacitance of the gate stack, C_{tot} then results from the combination in series of the low-κ (l- κ) and high-κ (h- κ) dielectric layer capacitances, i.e.

$$\frac{1}{C_{tot}} = \frac{1}{C_{low-\kappa}} + \frac{1}{C_{high-\kappa}} \tag{1.3}$$

The equivalent oxide thickness then reads

$$EOT = \frac{\varepsilon_{r,SiO_2}}{\varepsilon_{r,l-\kappa}} t_{h-\kappa} + \frac{\varepsilon_{r,SiO_2}}{\varepsilon_{r,h-\kappa}} t_{h-\kappa}$$

$$EOT = EOT_{low-\kappa} + EOT_{high-\kappa}$$

$$EOT = t_{\text{int}} + EOT_{high-\kappa}, \tag{1.4}$$

the presence of the low-κ interfacial layer increases the equivalent oxide thickness of the gate stacks (Fig.1.5), and should be as thin as possible to achieve the equivalent oxide thickness (EOT) required by the ITRS.

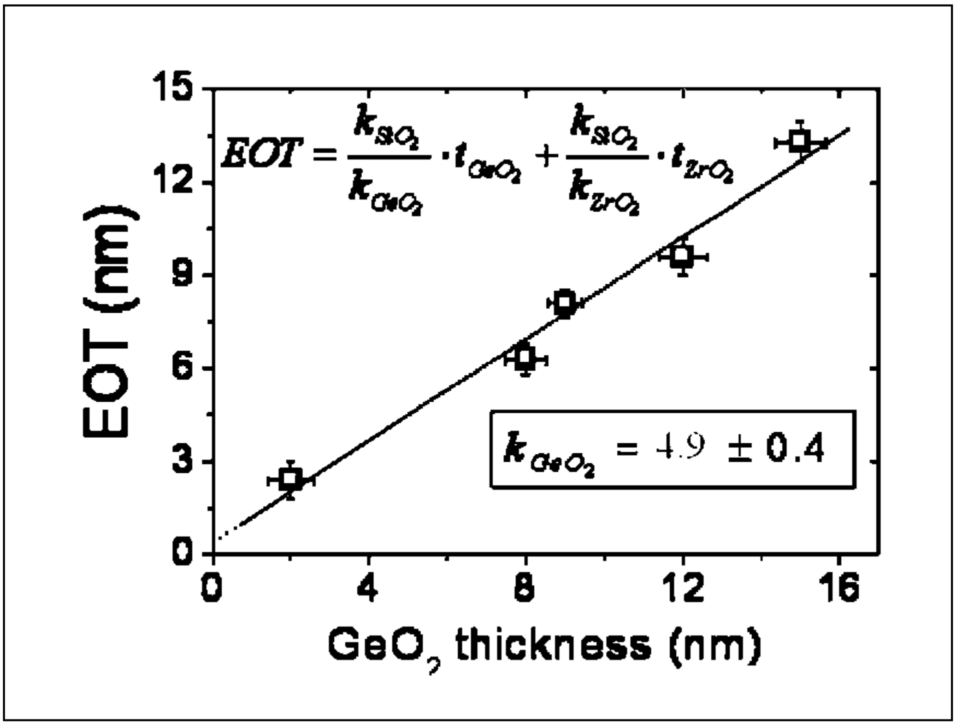

Fig. 1.5: *EOT as a function of t_{ox} for samples with 2nmZrO$_2$/GeO$_2$/n-Ge structures. The κ-value of GeO$_2$ is found around ~ 4.9 and κ-value for ZrO$_2$ (tetragonal phase) around 44. After Ref. [22].*

A lot of effort focused on the investigation of high-κ gate dielectrics, for the potential replacements of SiO$_2$ in advanced CMOS technologies. A list of materials studied in the literature is given in *Table 1.1* together with their relative dielectric constants.

Table 1.1: *Examples of high-κ materials studied in the literature for the potential replacement of SiO_2 as advanced gate dielectrics. After Ref. [20].*

Material	**Dielectric constant ε_r**	**Energy gap E_g(eV)**	**Material**	**Dielectric constant ε_r**	**Energy gap E_g(eV)**
Al_2O_3	**9-11**	**8.7**	**Dy_2O_3**	**11-14**	**-**
Ta_2O_5	**25-26**	**4.4**	**Nb_2O_5**	**11-14**	**-**
TiO_2	**50-80**	**3.05**	**Gd_2O_3**	**9-14**	**5.9**[b]
CeO_2	**21-50**	**3.3**[a]	**$SrTiO_4$**	**50**	**5.2**
$SrTiO_3$	**200**	**3.2**	**ZrO_2**	**14-25,44**[a]	**5.8**
Y_2O_3	**12-18**	**6.0**	**Si_3N_4**	**7.4**	**5.1**
HfO_2	**15-25**	**5.6**	**La_2O_3**	**21-30**	**5.7**

[a] *After Ref. [22]*
[b] *After Ref. [23]*

Since SiO_2 approached its physical limit, alternative dielectrics have been introduced, which meet stringent requirements including thermal stability, large band gap, and compatibility to conventional CMOS process. Moderate dielectric constant (κ) materials (15~30) were preferred due to fringing field induced barrier lowering. It was reported that a universal relation between κ value and breakdown properties. In general, as κ increases, barrier height and breakdown strength decreases (Fig.1.6). A material structure plays an important role of breakdown of the high-κ dielectrics. In addition, different charge fluence by different barrier height changes breakdown properties as well.

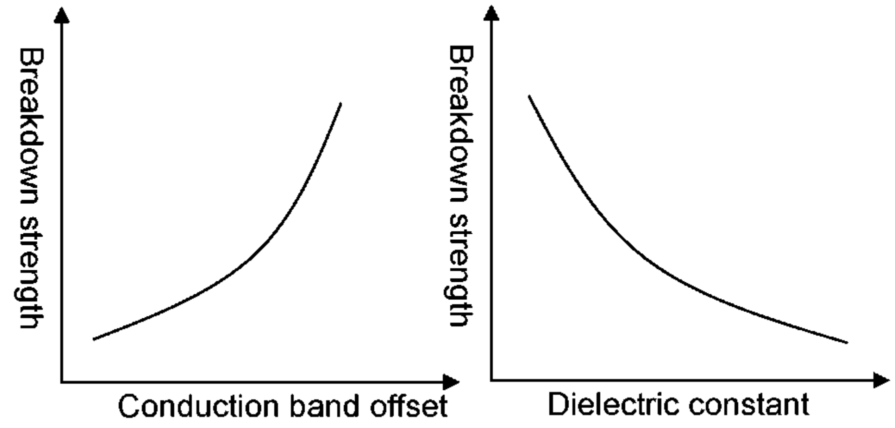

Fig. 1.6: *A universal relation between band offset and breakdown strength.*

1.4 Using REOs as dielectrics (interfacial passivation layer)

High mobility Germanium metal oxide field effect transistors with high-*κ* gates are considered to be good candidates for high performance applications. To develop a viable Ge MOS technology, the main challenge is to have better Ge surface passivation methodology and identify appropriate high-k gate dielectrics to combine oxide scaling below 1 nm with good electrical quality of the interfaces as well as reliability aspects.

High-*κ* dielectrics, for example, HfO_2 deposited directly on Ge gives sharp interfaces (1.7 (b)) [21] however the electrical behavior is very poor. One of the solutions could be the use of the dielectric together with an interfacial layer (IL) to form gate stack. The gate stack must combine good potential for scaling with good device performance characteristics which is perhaps the most challenging issue in Ge technology. Different efforts have been demonstrated as a passivation interfacial layer, such as, GeON [24], GeO_2 [25] to form gate stacks on Ge surface. It has also been demonstrated on the basis of MOS capacitors that HfO_2, ZrO_2 with these IL are thermally stable [26-27] and have good potential for scaling giving equivalent oxide thickness (EOT) well below 1 nm [28-29] and J_g below 1 A/cm^2 the latter being several orders of magnitude lower than that of HfO_2/Si and SiO_2/Si systems.

An alternative approach to the passivation problem could be the use of rare earth oxides [30] A number of these oxides such as La_2O_3, CeO_2, Gd_2O_3, Dy_2O_3 can be deposited directly on Ge with improved electrical characteristics, i.e., these oxides are friendly with Ge producing well behaving device characteristics, especially in metal-insulator- semiconductor (MIS) capacitors, and giving good passivation characteristics. A possible reason for this behavior is that rare earth oxides react strongly with the substrate resulting in catalytic oxidation of Ge and in the spontaneous formation of stable interfacial layers.

In the case of CeO_2, a significant reduction of D_{it} in the $10^{11}eV^{-1}cm^{-2}$ range is observed. This is a substantial improvement with respect to MBD-prepared HfO_2/GeON gates. On the other hand, CeO_2 suffers from leakage since it has a low band gap of about 3.3 eV [23]. In addition, an interfacial layer (IL) is spontaneously formed [Fig. 1.7(a)] increasing with film thickness and deposition temperature [21] which makes gate scaling difficult. Despite of that, MIS capacitors suffer from high leakage [31] due to the low energy gap of CeO_2 raising concerns about its scalability to low equivalent oxide thickness (EOT) values. Gd_2O_3 has attracted interest mainly because it can be grown in crystalline form on Ge with abrupt interfaces [32]. However, there is not enough evidence at the moment about its dielectric quality and its suitability as a gate dielectric for Ge devices. For the case of La_2O_3, Ge diffuses in the oxide film most probably resulting in intermixing of La–O [Fig. 1.7(c)] with the substrate [33]. At the same time, D_2O_3 shows good passivation properties when deposited on Ge substrates [34-35]. Using CeO_2, La_2O_3, or Dy_2O_3 as ultrathin passivating layer and combining it with HfO_2 cap, leakage is improved resulting in long channel functional *p*- and *n*-FETs, reduce the interface defect-assisted generation of minority carriers, and also improve electrical characteristics [33-36].

It has been drawn more attention, in particular, on the properties of artificially and spontaneously formed interfacial layers [21]. Two types of interfaces had been examined.

The first is a non-reacting one made by direct deposition of HfO_2 on Ge by MBD. The main characteristics are atomically sharp interface with no sign of oxidized Ge as inferred from XPS and negligible Ge diffusion in the HfO_2 when the deposition temperature is kept sufficiently low. However, samples with abrupt interfaces give poor electrical (*C–V and I–V*) characteristics. The *C–V* characteristics can be partly recovered by artificial formation of a thin GeON passivating layer [2-3], despite the fact that this layer is unstable in contact with overlaying HfO_2, and after dissociating (at least in part) allows Ge to diffuse in the HfO_2. Although GeON interfacial layers are beneficial [24], *C–V* and *G–V* characteristics remain far from ideal exhibiting large hysteresis, strong frequency dispersion, particularly in inversion, and high density of interface states D_{it}. The second type of interfaces examined is a strongly reacting interface between the rare earth CeO_2 and Ge, producing spontaneously (during deposition) an interfacial layer which contains oxidized Ge [4]. In contrast to GeON/HfO_2, the interfacial layer in the CeO_2/Ge system is stable showing limited Ge diffusion in HfO_2 when the deposition temperature is kept sufficiently low [21]. CeO_2/Ge metal insulator semiconductor capacitors show improved C–V characteristics compared to GeON/ HfO_2 with very small frequency dispersion, much reduced hysteresis and D_{it} around 1×10^{12} eV^{-1} cm^{-2} [4]. Several other rare earth oxides (La_2O_3, Dy_2O_3 and Gd_2O_3) can be deposited directly on Ge without an artificially made interfacial layer and this also shows improved electrical behavior.

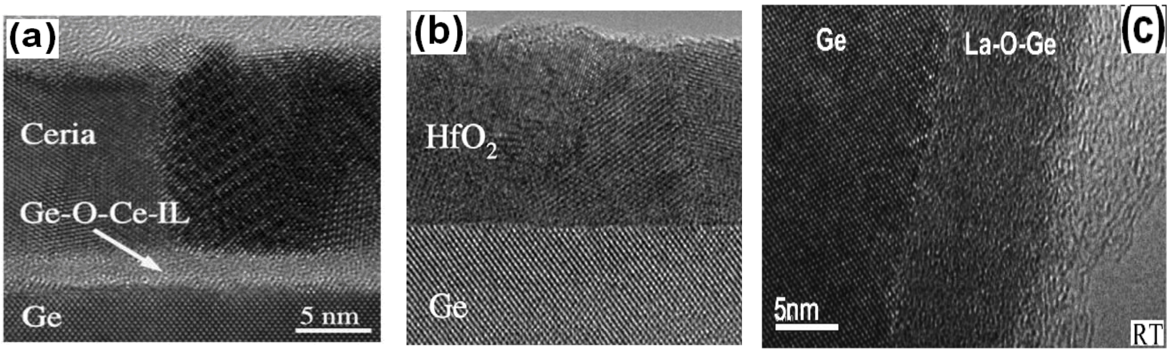

Fig. 1.7 : *Cross-sectional TEM micrograph showing* ***(a)*** *ceria(CeO_2) dielectric* ***(b)*** *HfO_2, and* ***(c)*** *La_2O_3 deposited directly on a clean Ge surface at a temperature Td=225°C (a)-(b) and (c) at room temperature. The brighter contrast shows the interfacial layer (see (a)) which is formed spontaneously during the deposition of ceria, while for HfO2 is non-reacting interface (see (b)), while in (c) spontaneous formation of germanate (La-O-Ge). (a) & (b) After Ref. [33], (c) After Ref. [37].*

Suffering from high leakage current or low effective dielectric constant, these oxides cannot stand alone as gate dielectrics; however they could play the role of an efficient passivating layer in more complex gate stacks for future Ge devices. As a final concluding remark, we note that avoiding oxidation of Ge does not guarantee better passivated interfaces with improved electrical behavior. This is proven by the fact that interfaces free of oxidized Ge (such as those formed by direct deposition of HfO_2/Ge) show poor electrical behavior. In addition, the CeO_2/Ge system with a thick interface containing oxidized Ge shows significantly improved characteristics. Instead of trying to avoid Ge oxidation altogether, we should rather avoid germanium oxides in the wrong oxidation states. On the other hand, germanium oxide in the right oxidation state (either 2+ or 3+ according to XPS results [21] may provide a desirable passivating layer. This could be formed by identifying the right material to oxidize Ge perhaps through a catalytic reaction as in the case of ceria. This could lead to a new approach.

1.5 Metal-Oxide-Semiconductor (MOS)

1.5.1 Introduction

As the semiconductor industry strives for smaller and faster devices, many issues need to be addressed in order to reach targeted objectives. One major issue is the scaling of device dimensions. As lengths and widths reduce, film heights (thickness) must also reduce. One of these areas is the gate dielectric in a Metal-Oxide-Semiconductor (MOS) structure. The gate dielectric thickness is the smallest fabricated dimension in MOS transistors today. Electrical characterization of the MOS test structures is crucial in the development of future MOS devices and circuitry. The Metal-Oxide-Semiconductor (MOS) structure plays a significant role in MOS Field Effect Transistors (MOS FETs) which are prevalent in the integrated circuit technology of today. The MOS capacitor is the metal-insulator-semiconductor structure that creates the conductive channel in a MOSFET. With the use of semiconductor processing equipment, these structures can be fabricated together to form a parallel plate capacitor as shown in Fig. 1.8 where the metal gate and the semiconductor substrate form the metal plates and the insulator forms the dielectric between the two plates. These structures are used extensively in research as a process control that addresses the need for characterization of ultra-thin oxides and alternative gate dielectrics.

1.5.2 MOS structures

To do this research, a fundamental understanding of MOS materials is vital. One useful tool is the semiconductor band structure of these materials. Figure1.8 shows the ideal case of the MOS structure. In the ideal case, several assumptions have been made [38]: (i) there are no charges present in the dielectric film; (ii) the dielectric is a perfect insulator where no current can pass through under different biasing conditions; (iii) the semiconductor thickness must be large enough to contain a field free region in the bulk of the substrate despite the applied gate potential; (iv) the semiconductor is a uniformly doped substrate; and (v) the backside semiconductor-metal contact must be ohmic.

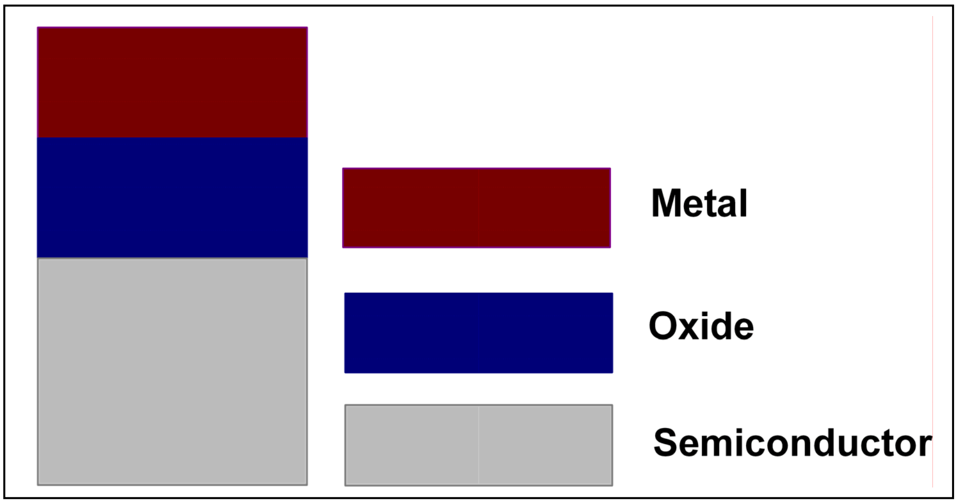

Fig. 1.8: *A MOS capacitor where the wine color shaded portion represents the metal electrode, the "navy blue" portion represents the insulating dielectric, and the light gray shaded portion represents the Germanium substrate. This forms a parallel plate capacitor.*

1.5.3 Band diagram of an ideal MOS Structure

Now that the assumptions have been given, static biasing issues can be addressed for metal serving as the gate electrode of the MOS capacitor. The four static biasing conditions that will be addressed are: accumulation, flatband, depletion (in the substrate), and inversion (in the substrate).

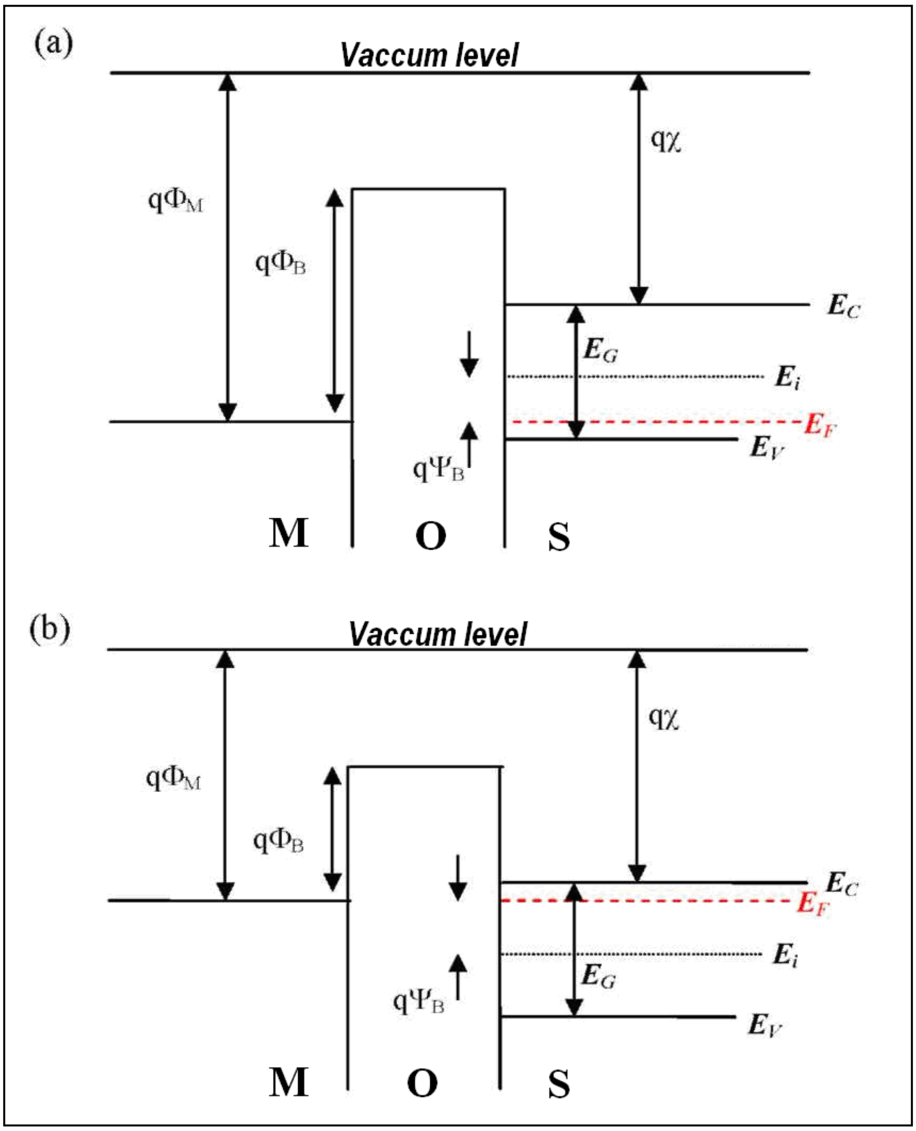
(a)
Vaccum level
qχ
qΦ_M
qΦ_B
E_C
E_G
E_i
E_F
E_V
qΨ_B
M
O
S
(b)
Vaccum level
qχ
qΦ_M
qΦ_B
E_C
E_F
E_i
E_G
E_V
qΨ_B
M
O
S

Fig. 1.9: *The energy band diagrams of an ideal (no oxide charges, perfect insulator, and uniformly doped substrate, V=0) MOS device with a (a) p-type semiconductor and (b) n-type semiconductor.*

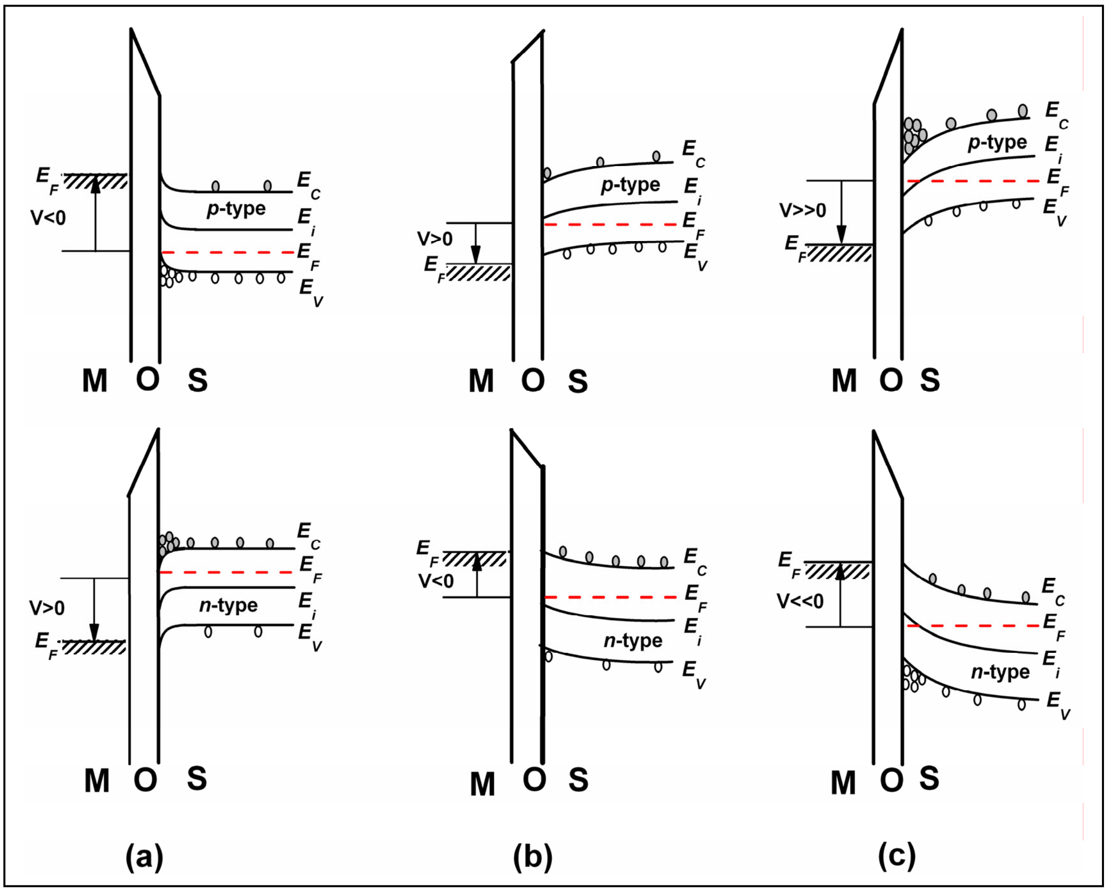
E_F
V<0
p-type
E_C
E_i
E_F
E_V
M O S
V>0
E_F
p-type
E_C
E_i
E_F
E_V
M O S
V>>0
E_F
p-type
E_C
E_i
E_F
E_V
M O S
V>0
E_F
n-type
E_C
E_F
E_i
E_V
M O S
E_F
V<0
n-type
E_C
E_F
E_i
E_V
M O S
E_F
V<<0
n-type
E_C
E_F
E_i
E_V
M O S
(a)
(b)
(c)

Fig. 1.10: *Energy-band diagrams for ideal MOS capacitors under different bias, for the conditions of: (a) accumulation, (b) depletion, and (c) inversion. Top/bottom figures are for p-type /n-type semiconductor substrates.*

1.5.4 Qualitative Description

In the scenario presented, the substrate is at ground and the bias is applied to the metal gate. In this situation, the semiconductor Fermi level, E_{Fs} is at ground potential, and the metal gate Fermi level, E_{Fm}, can be considered as a "handle" that moves up for negative applied bias and down for a positive applied bias. Another important parameter to discuss is the metal-semiconductor work function, Φ_{ms}. The work function of any materials is in units of electron volts (eV) and is defined as the distance from the Fermi level to the vacuum level for a given material (Fig. 1.9). The metal-semiconductor work function is the difference of the metal work function (Φ_m) from that of the semiconductor (Φ_s). Thus,

$$\Phi_{ms} = \Phi_m - \Phi_s \tag{1.5}$$

1.5.5 Flatband

The flatband voltage is the voltage required to make the bands horizontal (i.e., with no band bending) as shown in Fig. 1.9 (a) and (b). Using the assumption that no charges are present in the oxide, the flatband voltage can be positive or negative depending on the value of Φ_m relative to Φ_s, as demonstrated in Fig. 1.11(c).

1.5.6 Accumulation

For both p/n-type MOS structures, accumulation occurs when a negative/positive bias is applied to the gate. The negative charges on the gate attract holes to the high-κ/substrate (e.g. Dy_2O_3/p-Ge or CeO_2/n-Ge) interface to form an accumulation layer (see Fig. 1.11(b)).

The band structure also undergoes a change from the previous static bias condition to the Figure 1.10(a) for both p/n-type substrates. When the negative/positive bias is applied to the gate, the Fermi level moves up/down relative to the grounded Fermi level in the substrate creating the band bending shown.

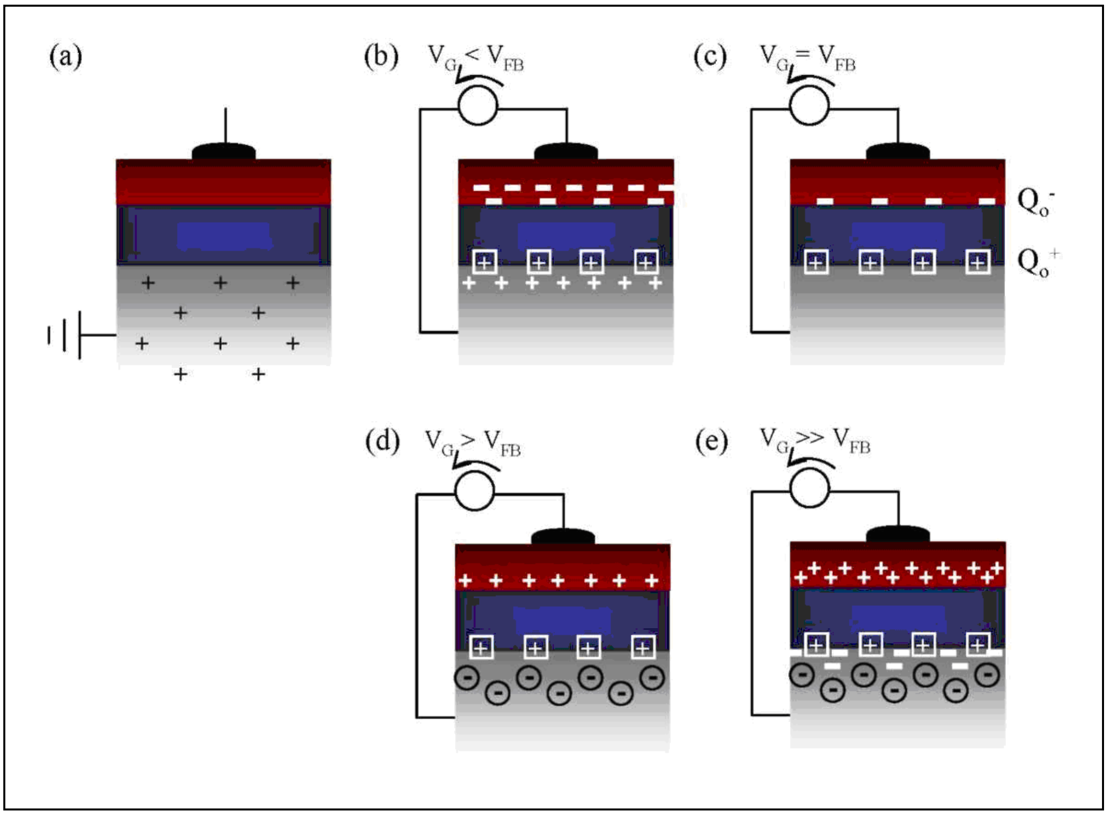

Fig. 1.11 (a)-(e): *The metal-oxide semiconductor capacitor (MOSCAP) in (a) standby [no bias], (b) accumulation [*$V_g<V_{FB}$*], (c) flatband [*$V_g=V_{FB}$*], (d) depletion [*$V_g>V_{FB}$*], and (e) inversion [*$V_g>>V_{FB}$*].*

1.5.7 Depletion

As the bias increases from a negative/positive accumulation bias, holes/electron begin to leave the high-κ/substrate (e.g. Dy_2O_3/Ge or CeO_2/Ge) interface until the flatband condition is reached. Continuing to increase the bias begins to deplete holes/electrons at the interface as well as a certain distance into the p/n-type substrate forming a depletion region shown in Fig. 1.11(d).

The band structure also undergoes a change from a previous static bias condition to Figure 1.10(b) for both p/n-type substrates. When the increasing bias is applied to the gate the Fermi level moves downward/upward relative to the grounded Fermi level in the substrate creating the band bending shown.

1.5.8 Inversion

As the bias continues to increase from a depletion bias, assuming sufficient inversion charge is established (which could take some time), a maximum depletion width is established, and then, electrons/holes begin to move towards the high-κ/substrates (e.g. Dy_2O_3/p-Ge or CeO_2/n-Ge) interface to form an inversion layer as shown in Fig. 1.11(e).

The band structure also undergoes a change as shown Figure 1.10(c) for *p/n*-type substrates. When the increasing bias is applied to the gate, the Fermi level continues to move downward/upward relative to the grounded Fermi level in the substrate creating the band bending shown.

1.5.9 Surface Space-Charge Region

In this section we derive the relations between the surface potential, space charge, and electric field. These relations are then used to derive the capacitance-voltage characteristics of the ideal MOS structure in the following section.

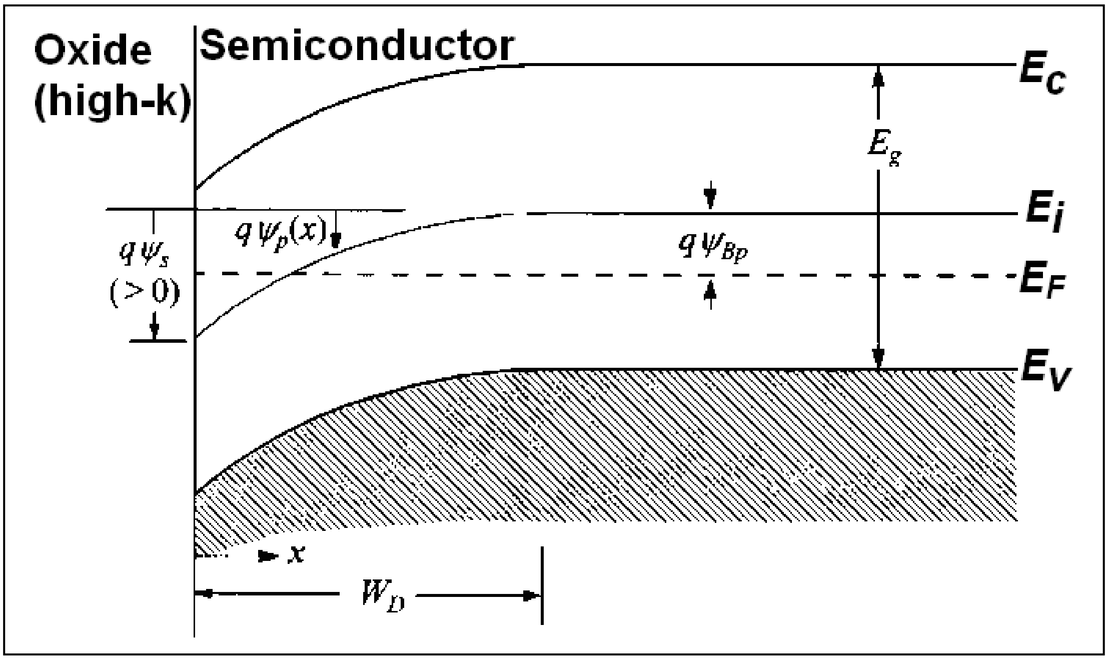

Fig. 1.12: *Energy-band diagram at the surface of a p-type semiconductor. The potential energy* $q\Psi_p$ *is measured with respect to the intrinsic Fermi level* E_i *in the bulk, while* W_D *is the depletion width. The surface potential* Ψ_S *is positive as shown. Accumulation occurs when* $\Psi_S<0$*. Depletion occurs when* $\Psi_{Bp} > \Psi_S > 0$*. Inversion occurs when* $\Psi_S > \Psi_{Bp}$*.*

Figure 1.12 shows a more detailed band diagram at the surface of a *p*-type semiconductor. The potential $\Psi_p(x)$ is defined as the potential $E_i(x)/q$ with respect to the bulk of the semiconductor,

$$\psi_p(x) = \frac{[E_i(x) - E_i(\infty)]}{q} \quad (1.6)$$

At the semiconductor surface, $\Psi_p(x)=\Psi_S$, and Ψ_S is called the surface potential. The electron and hole concentrations as a function of Ψ_S are given by the following relations:

$$n_p(x) = n_{po} \exp\left(\frac{q\psi_p}{kT}\right) = n_{po} \exp(\beta\psi_p) \tag{1.7}$$

$$p_p(x) = p_{po} \exp\left(\frac{-q\psi_p}{kT}\right) = p_{po} \exp(-\beta\psi_p) \tag{1.8}$$

where Ψ_p is positive when the band is bent downward (as shown in Fig. 1.12), n_{po} and p_{po} are the equilibrium densities of electrons and holes, respectively, in the bulk of the semiconductor, and $\beta=q/kT$.

From previous discussions and with the help of the above equations (1.5, 1.6, 1.7, and 1.8), the following regions of surface potential can be distinguished:

$\Psi_S < 0$ Accumulation of holes (band bending upward)

$\Psi_S = 0$ Flat-band condition.

$\Psi_{Bp} > \Psi_S > 0$ Depletion of holes (band bending downward)

$\Psi_S = \Psi_{Bp}$ Fermi-level at midgap, $E_F=E_i(0)$, $n_p(0)=p_p(0)=n_i$

$2\Psi_{Bp} > \Psi_S > \Psi_{Bp}$ Weak inversion [electron enhancement, $N_A > n_p(0) > p_p(0)$]

$\Psi_S > 2\Psi_{Bp}$ Strong inversion [electron enhancement, $n_p(0) > N_A$]

1.6 Capacitance-Voltage (C-V) characteristic

The Capacitance-Voltage behavior of a MOS device can be described using the equivalent circuit shown in Fig. 1.13 [39] where C_{OX} is the oxide capacitance, C_S the substrate capacitance, C_{it} the interface state capacitance, R_S the series resistance and $1/R_P$ the parallel conductance.

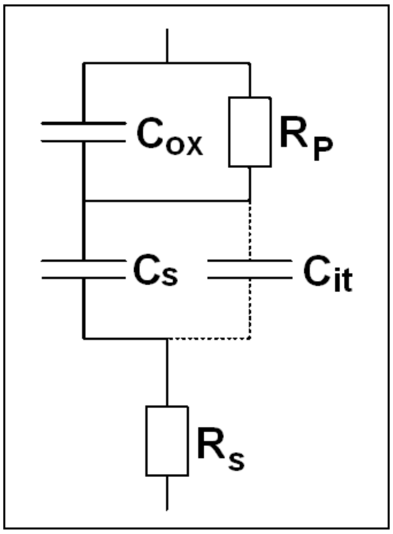

Fig. 1.13: *Equivalent circuit of an MOS structure including the oxide capacitance (C_{OX}), the substrate capacitance (C_S), interface state capacitance (C_{it}), series resistance (R_S) and parallel conductance ($1/R_P$).*

The capacitance of a MOS capacitor is defined as

$$C = \frac{dQ_g}{dV_g} \tag{1.9}$$

Based on charge neutrality $Q_g = -(Q_S + Q_{it})$ where Q_S, the substrate charge, and Q_{it}, the trapped interface charge. This assumes no charge trapping in the dielectric. The gate voltage is partially dropped across the dielectric and partially across the semiconductor substrate. This gives

$$V_g = V_{FB} + V_{OX} + \phi_S, \tag{1.10}$$

where V_{FB} is the flatband voltage, V_{OX} the voltage drop across the oxide and ϕ_S the Ge surface potential allowing Eq. 1.1 to be written as

$$C = \frac{dQ_S + dQ_{it}}{dV_{OX} + d\phi_S}, \tag{1.11}$$

Depending on the Ge surface potential either majority, minority or depletion charge is contributing to the substrate charge. The total gate capacitance can now be written as

$$C = \frac{1}{\frac{1}{C_{OX}} + \frac{1}{C_S + C_{it}}} \tag{1.12}$$

The low − frequency substrate capacitance is given by

$$C_{S,lf} = \hat{U}_S \frac{\varepsilon_S \varepsilon_0}{2L_{Di}} \frac{\left[e^{U_F}\left(1 - e^{-U_S}\right) + e^{-U_F}\left(e^{U_S} - 1\right)\right]}{F\left(U_S, U_F\right)} \tag{1.13}$$

where the dimensionless surface electric field $F(U_S, U_F)$ is defined by

$$F(U_S, U_F) = \sqrt{e^{U_F}(e^{-U_S} + U_S - 1) + e^{-U_F}(e^{U_S} - U_S - 1)} \tag{1.14}$$

U_S and U_F are normalized potentials, defined as $U_S = q\phi_S / kT$, and $U_F = q\phi_F / kT$. The Fermi potential is calculated by, $\phi_F = (kT/q)\ln(N_A/n_i)$, where N_A is the acceptor concentration and n_i the intrinsic carrier concentration in the Ge substrate. The symbol $\hat{U}_S$ stands for the sign of the surface potential and is given by

$$\hat{U}_S = \frac{|U_S|}{U_S} \tag{1.15}$$

where $\hat{U}_S = 1$ for $U_S > 0$ and $\hat{U}_S = -1$ for $U_S < 0$. The extrinsic Debye length L_{Di} is

$$L_{Di} = \sqrt{\frac{\varepsilon_S \varepsilon_0 kT}{2q^2 n_i}} \tag{1.16}$$

The high-frequency C-V curve results when the minority carriers in the inversion charge are unable to follow the ac voltage. The majority carriers at the semiconductor edge are able to follow to the ac signal thereby exposing more or less ionized dopants atoms. The high – frequency semiconductor capacitance in inversion is [40]

$$C_{S,hf} = \hat{U}_S \frac{\varepsilon_S \varepsilon_0}{2L_{Di}} \frac{\left[e^{U_F}\left(1 - e^{-U_S}\right) + e^{-U_F}\left(e^{U_S} - 1\right)\right]/(1+\delta)}{F\left(U_S, U_F\right)}, \tag{1.17}$$

with δ given by

$$\delta = \frac{\left(e^{U_S} - U_S - 1\right) / F\left(U_S, U_F\right)}{\int_0^{U_S} \frac{e^{U_F}\left(1 - e^{-U}\right)\left(e^{U} - U - 1\right)}{2\left[F\left(U_S, U_F\right)\right]^3} dU}, \tag{1.18}$$

1.6.1 High–low Capacitance-Voltage (C-V) characteristic curves

With a sufficiently negative and positive voltage, an accumulation and inversion layer is obtained in the MOS structure. Figure 1.12 shows the characteristic low-frequency and high-frequency trends of the capacitance as a function of applied gate voltage. At high frequencies, the minority carrier is unable to respond, and the majority carriers are able to respond in negative gate bias, or accumulation.

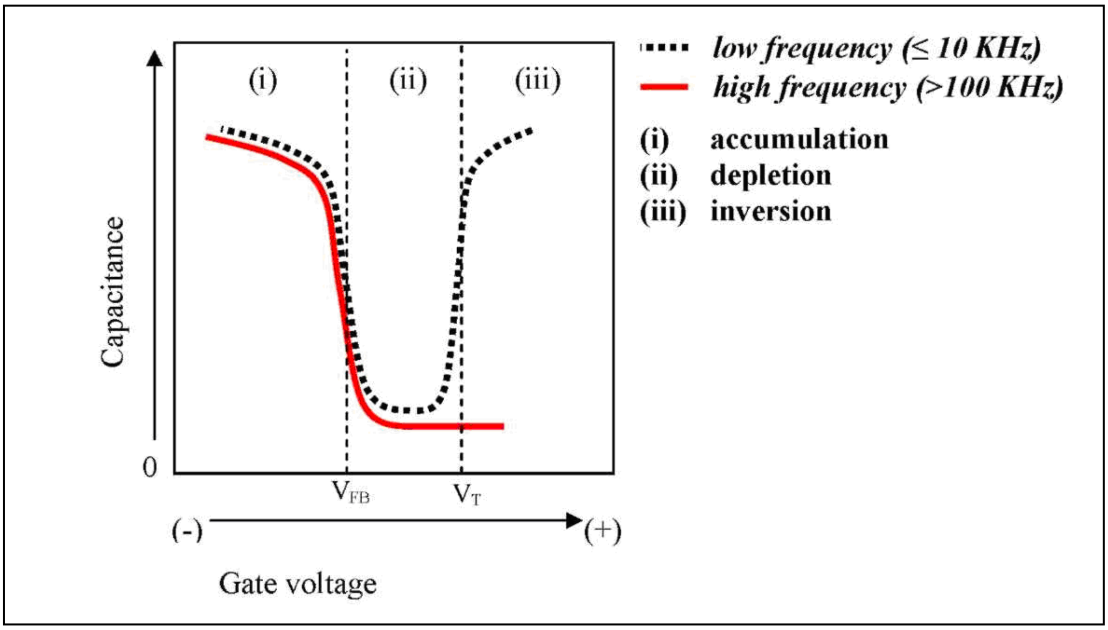

Fig. 1.14: *The three operating regions of the device shown for a capacitance-voltage (CV) measurement of an MOS device at a low measurement frequency (<10 kHz, black-dashed line) and a high measurement frequency (> 100 kHz, red line).*

1.6.2 Frequency dispersion of C-V characteristics

1.6.2.1 Frequency dispersion at accumulation

There are several mechanisms which may cause the dispersion of the capacitance with frequency observed (Fig. 1.15) at accumulation: (i) series resistances [41], (ii) parasitic effects in cluding back contact imperfection [42-43],(iii) a κ-value dependence on frequency of the interfacial dielectric layer [44]. To obtain the intrinsic properties and permittivity of the REOs dielectric from the *C-V* measurements, the

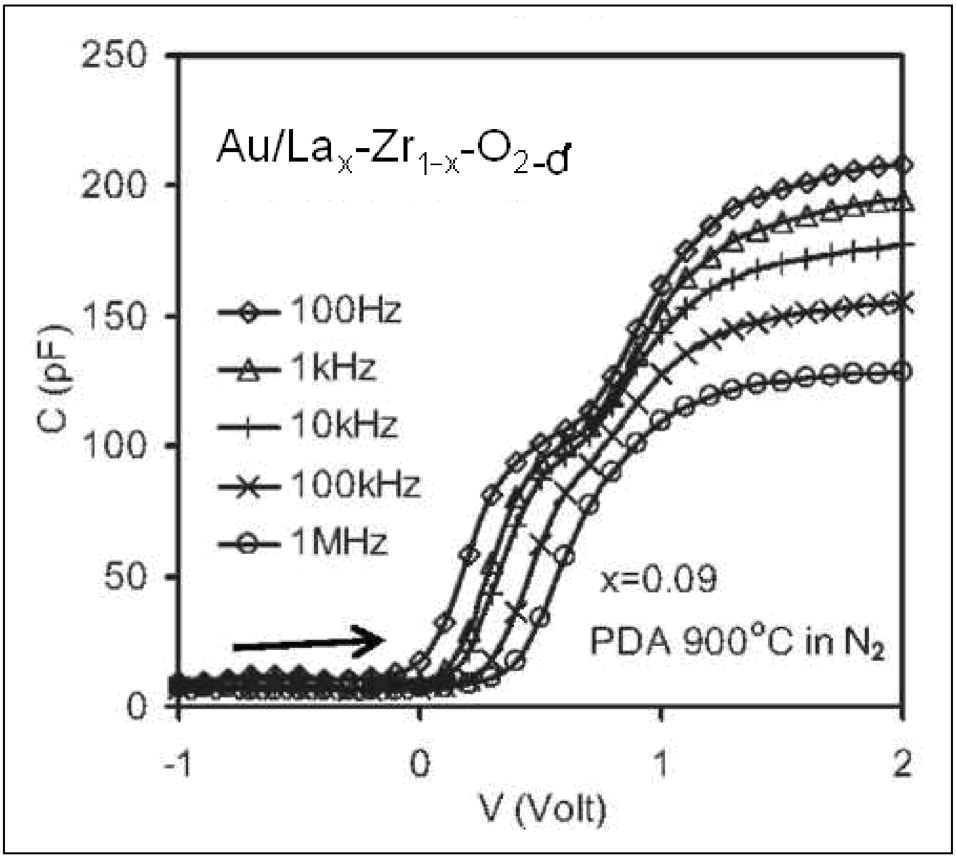

Fig. 1.15: *C-V results at different frequencies from the annealed sample Au/*La_x*-*Zr_{1-x}*-*$O_{2-\delta}$*/p-Si for x=0.09. Significant frequency dispersion at accumulation was observed. After Ref. [45]*

above mentioned effects must be eliminated. To reduce the effects of series resistance, back contacts (e.g. In-Ga alloy) can be deposited over a large area of the substrate wafer, which suppresses the effect of series resistances and back contact imperfections [42]. Cables and connections must be kept short to further minimize parasitic effects [43] as well.

1.6.2.2 Frequency dispersion at inversion

Germanium MOSFETs with high-κ dielectric gates could be good alternatives for future high performance logic devices due to the (low field) high carrier mobility [46]. The low frequency behaviour of the high frequency capacitance-voltage (C-V) curves (see Fig. 1.16), or more specifically, the observation of a high ac inversion

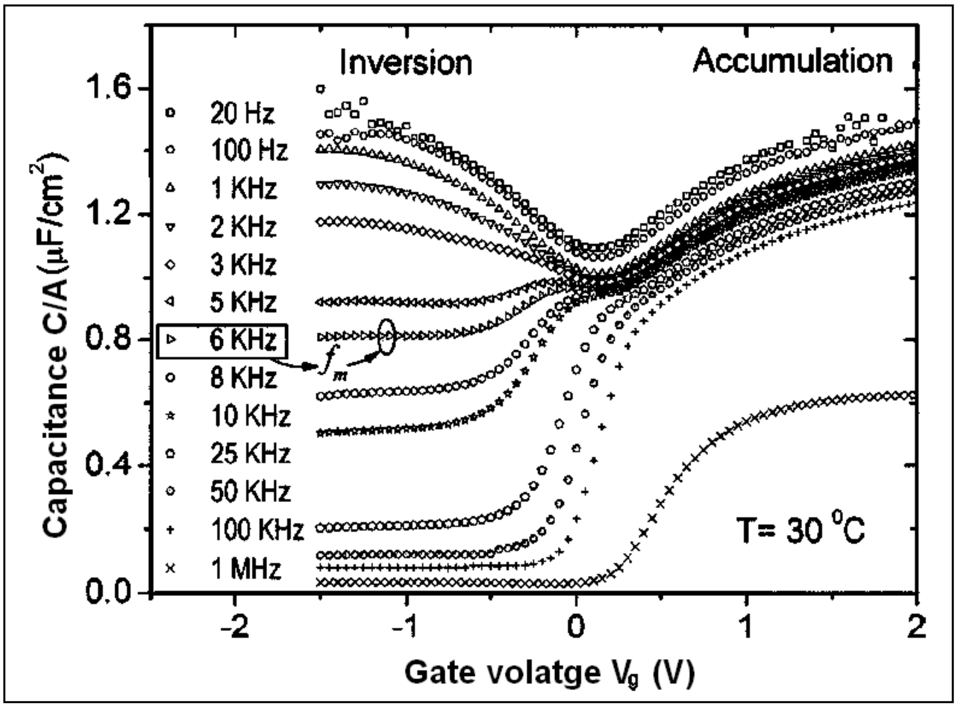

Fig. 1.16: *Room temperature C-V characteristics of an n type Pt/HfO$_2$/n-Ge MOS measured at different frequencies from 20 Hz to 1 MHz. Large frequency dispersion is observed at inversion (negative Vg). The transition frequency f_m, 6 kHz defined as the frequency at which the inversion capacitance is midway between low and high values, marks the transition from a low to high frequency behavior. After Ref. [48]*

capacitance [47] (close to the oxide capacitance value C_{ox}) at high frequencies (in kHz range) which is not expected based on the experience we have with device quality Si. This behaviour is usually attributed to contamination [47, 49] due to poor quality of bulk Ge starting material or due to insufficient surface passivation which creates high density of interface traps or mid-gap bulk semiconductor traps through metal diffusion from the high-κ over layer. These traps are considered to mediate the creation of electron-hole pairs in the depletion to provide the necessary seed of minority carriers which are necessary to built the inversion layer and give the high value of capacitance. The density of minority carriers in Ge though is expected to be higher compared to Si due to the lower energy gap (or higher intrinsic carrier concentration n_i). This could induce low frequency behaviour in Ge at high frequencies. As a matter of fact, Nicollian and Brews [41], had already predicted long before about this behaviour. f_m defined [41] as the frequency at which the capacitance in inversion is midway between high C_{inv} (20 Hz) and low C_{HF} values, marking the transition from low frequency to high frequency behavior.

Due to the short minority carriers' response time in Ge, an inversion layer is formed fast in response to an external ac signal at the gate, so that a high capacitance, equal to C_{ox} is formed even at high frequencies i.e., (1 kHz).

1.7 Interface state characterization

1.7. 1 Introduction

Next to the leakage current, the single most important metric for determining the usefulness of new gate dielectrics is the interface trap state density (D_{it}). The presence of interface states in a MOS device leads to several undesirable behaviors. First, the presence of any charge, whether it be at the interface or in the oxide itself leads to a shift in the capacitance voltage

(*C*-*V*) characteristics of the device. In a MOSFET, this directly translates to a change in threshold voltage. Second, since interface traps fill and empty with some characteristic time constant, there will be dispersion in the capacitance of the device as a function of frequency. Third, a large amount of trapped charge at the interface will degrade the channel mobility of a MOSFET via coulomb scattering of carriers. Finally, the sub-threshold current swing in a MOSFET is adversely affected by interface trap states. As a matter of fact, interface states are strongly correlated to the quality of the high-κ single dielectrics and/or gate stacks with semiconductor interlayer, and have been used as one of the primary parameters to characterize and monitor gate dielectric reliability.

1.7.2 Extraction of interface trap density (D_{it})

1.7.2.1 Theory

The first method for determining interface state density is the high-frequency capacitance method, also known as the Terman method, and in this method, the only measurement necessary is the high frequency (typically on the order of 1 MHz) capacitance versus voltage (*C*-*V*) curve. Even though interface traps cannot fill and empty on the time scales used to measure the capacitance, they can respond to the quasi-static bias sweep used to produce the *C*-*V* curve. Figure 1.17 illustrates that as the Fermi level crosses through the interface state distribution at a semiconductor surface; a sheet charge at the surface is created that is directly proportional to either the number of empty interface states for donor-like traps or filled states for acceptor-like traps. Since this sheet charge will depend on the position of the Fermi level at the interface, it will depend on the surface potential Ψs, and thus the applied gate voltage. This voltage-dependent charge layer can have a pronounced effect on the *C*-*V* characteristics even though the traps at the surface are not filling and emptying in phase with the ac signal.

What the trap states will do is to change the gate voltage for which a given Ψ_S is obtained. Donor-like states are defined as positively charged when empty and acceptor-like states are defined as negatively charged when filled.

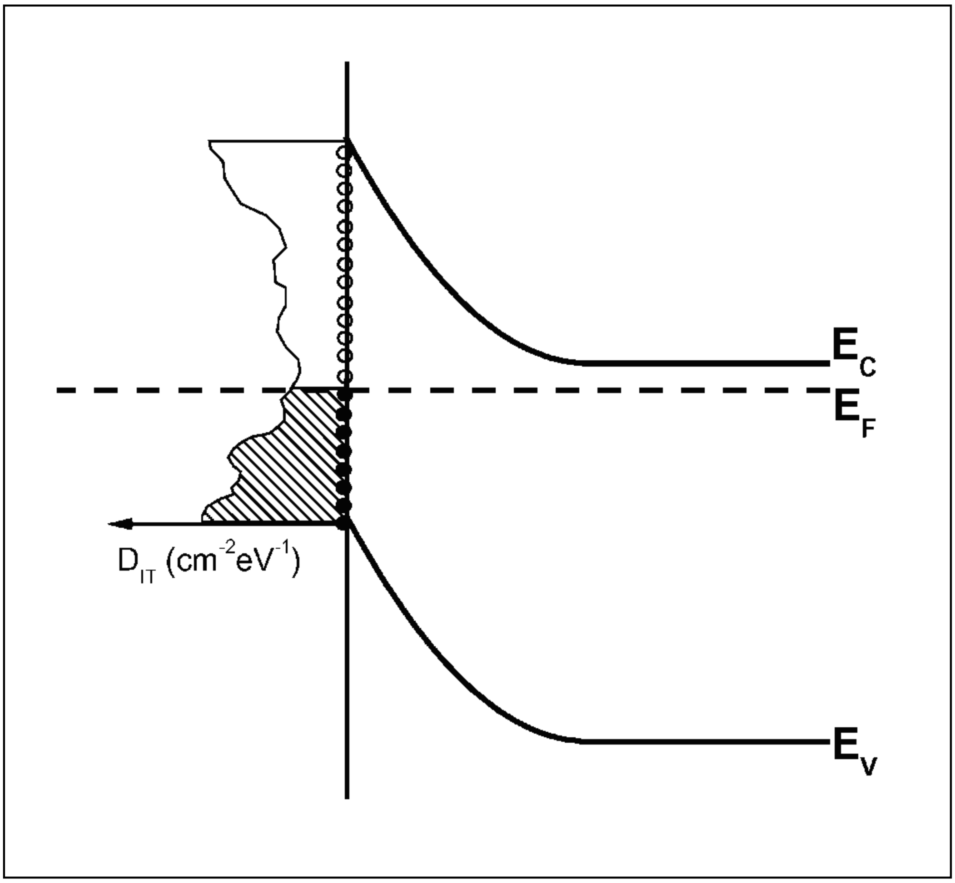

Figure 1.17: *Schematic of an insulator-semiconductor interface with interface states.*

At an insulator-semiconductor interface with dielectric constants, ε_{ox} and ε_S, and with a sheet charge δQ_{sheet} present at the interface, one of Maxwell's equations,

$$\nabla \bullet D = \rho \tag{1.19}$$

leads to the boundary condition

$$\varepsilon_{ox} E_{ox}^{\perp} - \varepsilon_S E_S^{\perp} = -Q_{sheet} \tag{1.20}$$

where the $\perp$ superscript implies the component of the electric field perpendicular to the interface. If Ψs is the potential at the semiconductor surface then boundary condition (1.20) becomes

$$C_{ox}(V_g - \Psi_S) - \varepsilon_S E_S^{\perp} = -Q_{sheet} \tag{1.21}$$

where $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the oxide capacitance, V_g is the applied gate bias, Q_{sheet} is any sheet charge located at the insulator-semiconductor interface, and Qs is the depletion/inversion charge in the semiconductor (Fig.1.18). Now we apply Gauss' law to an area just below the interface, from the semiconductor surface to beyond the depletion layer. The electric field entering the Gaussian box at the top is just $E_S^{\perp}$. Since the other side of the box is outside of the depletion region, the field leaving the box on the bottom is just zero. Because of symmetry in the direction parallel to the interface, there are no field lines leaving the sides of the box. Thus, Gauss' law gives

$$E_S^{\perp} = \frac{Q_S(\Phi_S)}{\varepsilon_S}, \tag{1.22}$$

where the Φs is included in order to emphasize the point that the semiconductor space charge is a function of the band bending. Now plugging (1.20) back into Eq. (1.19) we have,

$$C_{ox}(V_g - \Psi_S) = -Q_{sheet} - Q_S(\Phi_S) \tag{1.23}$$

In the case of a sheet charge generated by interface states, Q_{sheet} is also a function of Ψ_s as shown in Fig. 1.18. If Q_{sheet} is replaced by $Q_{it}(\Psi_S)$, V_g can be solved for, then differentiated with respect to Ψ_S to obtain

$$\frac{dV_g}{d\Psi_S} = 1 - \frac{1}{C_{ox}}\left(\frac{dQ_{it}}{d\Psi_S} + \frac{dQ_S}{d\Psi_S}\right) \tag{1.24}$$

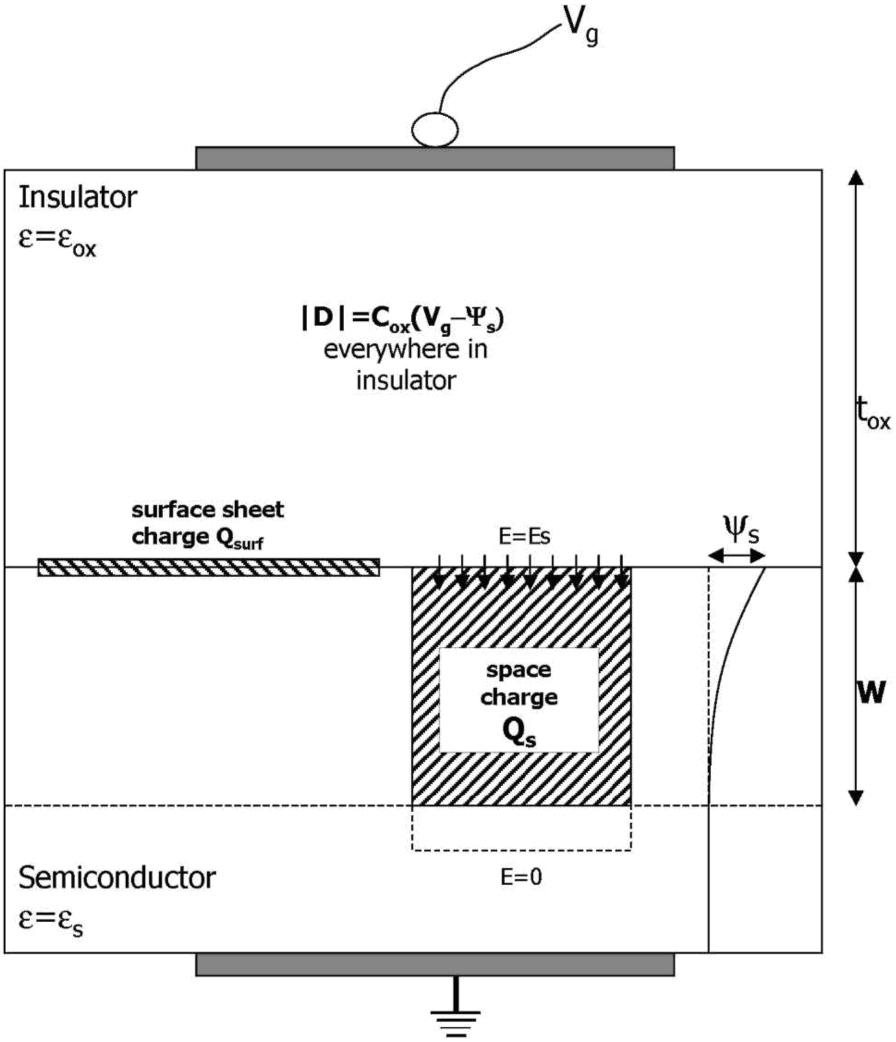
V_g
Insulator
ε=ε_ox
|D|=C_ox(V_g–Ψ_s)
everywhere in
insulator
t_ox
surface sheet
charge Q_surf
E=Es
Ψs
space
charge
Q_s
W
Semiconductor
ε=ε_s
E=0

Fig. 1.18: *Schematic of the important charges, fields and potentials at the insulator (oxide) semiconductor interface.*

The derivatives of the interface state charge and the semiconductor charge can be rewritten as capacitances, C_{it} and C_s, giving

$$C_{it} = C_{ox}\left(\frac{dV_g}{d\Psi_S} - 1\right) - C_S(\Psi_S) \qquad (1.25)$$

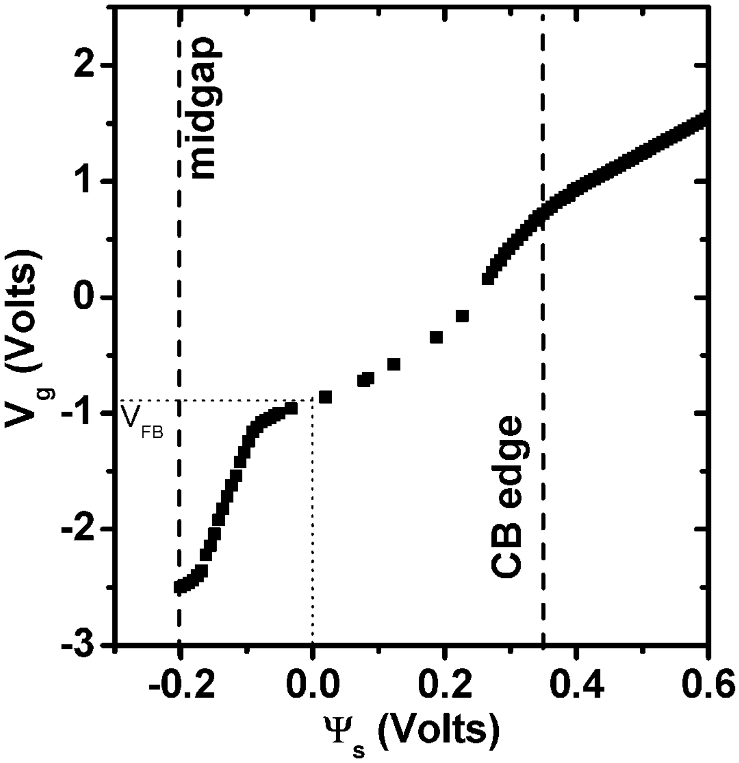

Fig. 1.19: *Example of a measured curve of V_g vs. Ψs. The derivative of this curve is used to compute the interface state density in the Terman method. This curve is also used to relate the position of the Fermi level within the germanium bandgap to the applied gate bias in both the Terman method and the conductance method.*

For an interface state density that is slowly varying throughout the energy gap relative to kT the interface state density can be approximated simply as $D_{it} = qC_{it}$ [41]. The important parameter to determine for this calculation is $dV_g / d\Psi_S$, which is an indication of how the band bending changes with applied gate voltage. The Terman method calculates this parameter as a function of Ψs by comparing an ideal theoretical *C-V* curve as a function of Ψs with the measured *C-V* curve. For each value of capacitance at a given Ψs in the theoretical curve, there is the corresponding value of capacitance at a given V_g in the measured curve. Thus it is possible to construct a curve of V_g vs. Ψs such as the one shown in Fig. 1.19.

In addition, conductance method [50] is widely being used for extracting density of interface states for high mobility Ge based MOS devices. Conductance can be written simply as a function of G_m, C_m, and C_{ox}, and:

$$G_t(\omega) = \frac{\omega^2 C_{ox} G_m}{G_m^2 + \omega^2 (C_m^2 - C_{ox}^2)}, \tag{1.26}$$

where C_{ox} can be measured directly in strong accumulation *i.e.*

$$C_{ox} = C_{ma}[1 + (G_{ma}/\omega C_{ma})], \tag{1.27}$$

is oxide capacitance and C_{ma} and G_{ma} are capacitance and conductance in accumulation, while $R_S = G_{ma}/[G_{ma}^2 + (\omega C_{ma})^2]$, ω the angular frequency, C_m and G_m are measured capacitance and conductance respectively. A plot of G_t/ω will be peaked as shown in Fig. 1.20. This peak can be thought of as occurring at a frequency for which the trap states are in "resonance" with the applied ac signal. At this frequency the highest possible numbers of traps are contributing to the conductance as described above. Thus the peak value of G_t/ω, which we will denote as $(G_t/\omega)_p$, should be roughly proportional to the interface trap density. However, statistical variations in the nature of the charge distribution under the gate cause fluctuations in the band-bending at the semiconductor surface. This can smear out the peaks and reduce their magnitude. The standard deviation of these fluctuations, σ_S, is related to the width of peak in the G_t/ω vs. ω curve and can be calculated from the data [41]. D_{it} is calculated approximately from the magnitude of the peak of G_t/ω curves at a given bias:

$$D_{it} \approx \frac{2.5}{q}\left(\frac{G_t}{\omega}\right)_p \tag{1.28}$$

where $\left(\frac{G_t}{\omega}\right)_p$ is the peak value from a $\left(\frac{G_t}{\omega}\right)$ vs. frequency ($\omega = 2\pi f$) plot.

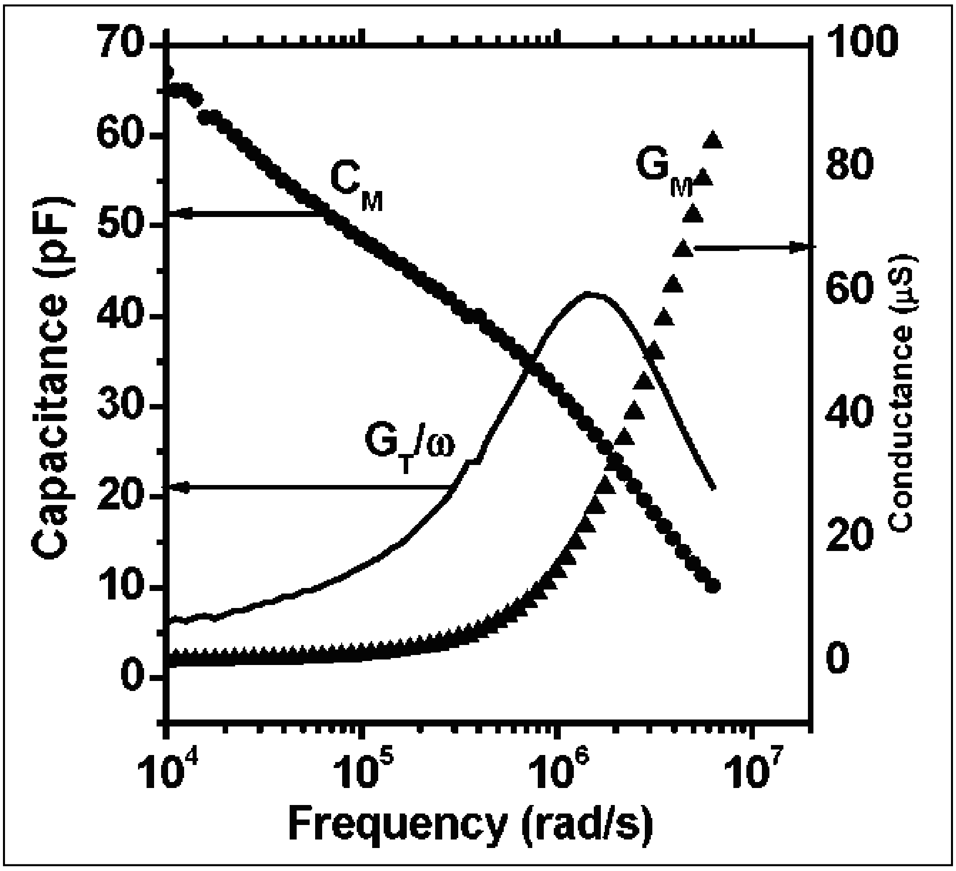

Fig. 1.20: The plot shows an example spectrum of the two measured quantities, G_m *and* C_m *along with the calculated spectrum of* G_t/ω *from Eq. (1.26).*

1.7.3 Types of Interface tarps

To determine the effect of interface traps on flatband, the type of interface trap has to be identified. There are two types of interface traps sitting in the bandgap; the charge state can be positive, negative or neutral, depending on their types or whether they are filled or empty. Detailed information is given in Table 1.2. Interface trap characteristics of thermal oxides are donor type in the upper half of the bandgap [41], no experiments on the donor or acceptor nature of interface traps in the lower half of the bandgap have been reported. If both donor and acceptor interface traps are present, a measured reduction in interface-trap-level density

$$D_{it} = D_{it}\,(donor) + D_{it}\,(acceptor) \qquad (1.29)$$

may be accompanied by a +/- shift in the flatband voltage. That is, elimination of donor interface traps reduces positive charge, whereas elimination of acceptor interface traps reduces negative charge. Therefore, the interface-trap-charge density

$$Q_{it} = Q_{it}\,(donor) - Q_{it}\,(acceptor) \tag{1.30}$$

may shift either way, depending on the charge balance of donor- and acceptor-type interface traps. Such a shift may mask any change in the oxide-fixed-charge density [41]. The important concern involved in this section is an interface-state-density extraction. No effort was made to investigate the types of interface states. It has to be kept in mind that a change in the interface-state density has no direct impact on the direction of flatband-voltage shift without the knowledge of the type of interface states.

Table 1.2: *The effect of interface traps on a C-V measurement*

Trap types	**Acceptor type**	**Donor type**
Filled by e	-ve charged	neutral
Empty	neutral	+ve charged
For p-substrate	Show more effect at depletion to inversion *region when the traps at the upper half of the bandgap change from empty to filled (neutral → -ve).*	Show more effect at depletion to accumulation *when the traps at the lower half of the bandgap change from filled to empty (neutral → +ve).*
For n-substrate	Show effect at dep→*acc.* Upper half bandgap empty→*filled* *(0→-ve)*	Show effect at dep→*inv* Lower half bandgap Filled→ empty *(0→+ve)*

1.7.4 D_{it} extraction techniques and conduction method

For MOS capacitors the choice for the most practical methods lies between *conductance* and *quasi-static* methods. These are the two most widely used techniques [39]. In order to extract the interface state density, the conductance model used by Nicollian and Goetzberger [50] was first fitted to the measured G/ω vs frequency curves at each voltage. Indeed, in a recent paper, Batude *et al.* [51] reports that the common D_{it} extraction techniques used for Si capacitors cannot be applied as such to Ge MOS structures.

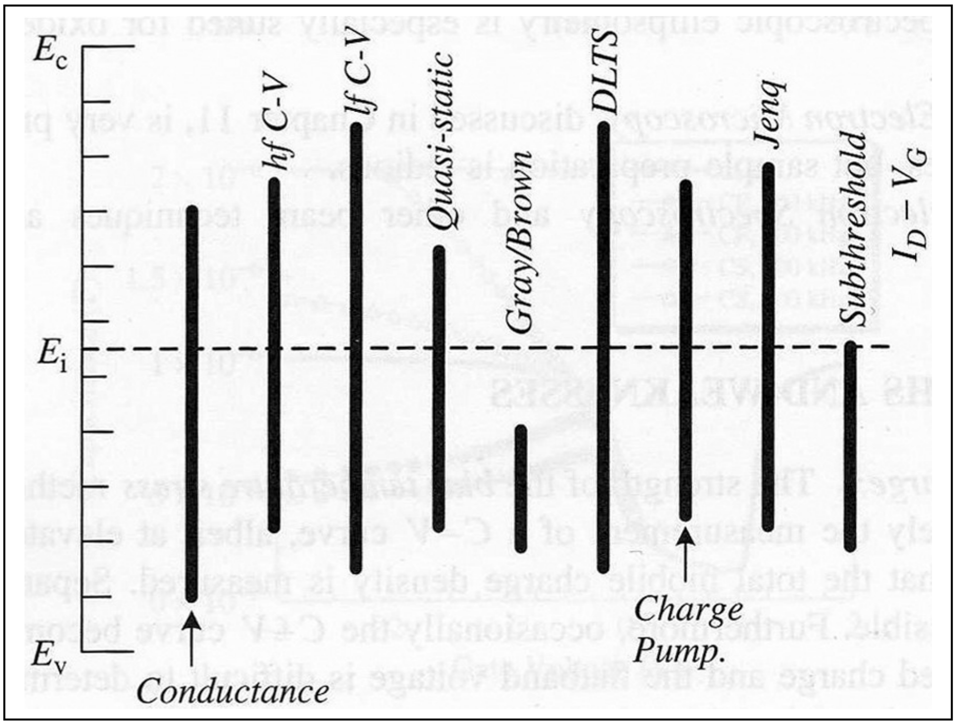
E_c
E_i
E_v
Conductance
hf C-V
lf C-V
Quasi-static
Gray/Brown
DLTS
Charge Pump.
Jenq
Subthreshold
$I_D - V_G$

Fig. 1.21: *Ranges of energy in the band gap of a p-type substrate over which interface trap changes are determined by various characterization techniques. After Ref. [39].*

It appears that weak inversion is a problem (due to the small bandgap of Ge) and a small density of impurities can generate large-frequency dispersion and high G/ω peaks, which should not be interpreted as large D_{it}. To avoid weak inversion in data interpretation, one can use the full conductance method with MOSFETs, as recently shown by Martens *et al.* [52]. In this method, the charge exchange between trap level (s) and both majority and minority carrier bands of the semiconductor, is taken into account.

From the above analysis of *C-V* characteristics at room temperature (T = 300 K), no flatband voltage shift was observed as a function of frequency [10]. Recently, IMEC group [25] demonstrated an extensive work on the D_{it} extraction techniques, in order to prove the effects of weak inversion as discussed above the *C-V* characteristics were also measured at low temperature ($T=77$ *K*). From room temperature (300K) and low temperature (77K) D_{it} values were reported 2×10^{11} $\mathrm{eV^{-1}cm^{-2}}$ and a few $10^{11}\mathrm{cm^{-2}eV^{-1}}$ for *n*-or *p*-Ge/GeO_2/HfO_2 respectively, which seems week inversion is not a problem *(as proposed by ref. [51])* to D_{it} extraction by conductance method.

1.8 Border traps (N_{bt}) characteristics

The concept of "border traps" was first proposed by D. M. Fleetwood in 1991[53]. Border traps are oxide traps that are able to exchange charge with the semiconductor substrates (e.g. Si, Ge) on the timescale of the electrical measurements. The ability to exchange charge with the substrate during the measurement makes border traps looks like interface traps electrically; however, the location of these defects are in the oxide, instead of at the interface (Fig. 1.22) [54]. Border traps are also termed as "near-interface traps" [55-57].

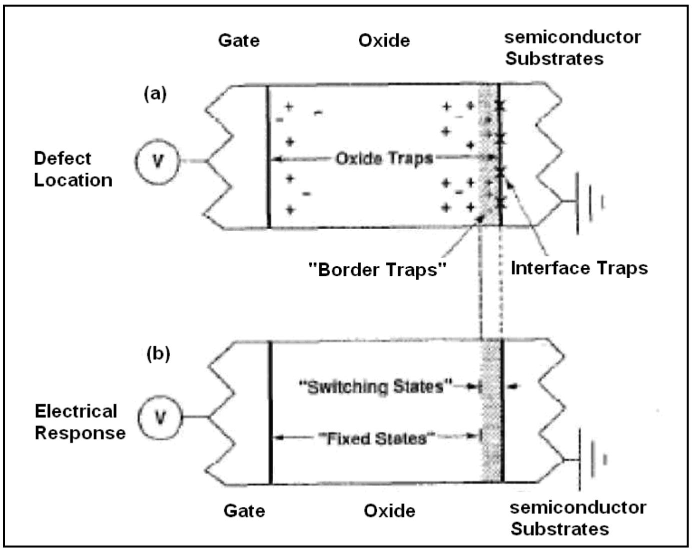
Gate
Oxide
semiconductor Substrates
(a)
Defect Location
V
Oxide Traps
"Border Traps"
Interface Traps
(b)
Electrical Response
V
"Switching States"
"Fixed States"
Gate
Oxide
semiconductor Substrates

Fig. 1.22: *Nomenclature that separates terms used to identify (a) defect location from (b) measured electrical response in MOS devices. The line between an oxide trap and a border trap depends on the time scale and bias conditions of the measurements. After Ref. [54].*

The microstructure of border traps is still under debate, with no single defect likely responsible for all border-trap effects in all materials and devices. In some devices, border traps are apparently associated with hydrogen-related defects in the near-interfacial SiO_2 [58-59], or other defects not directly associated with trapped holes [60-61]. Since border traps can sometimes be mistaken for interface traps electronically; separation of the contribution of border traps from real interface traps is performed in the study of charge trapping.

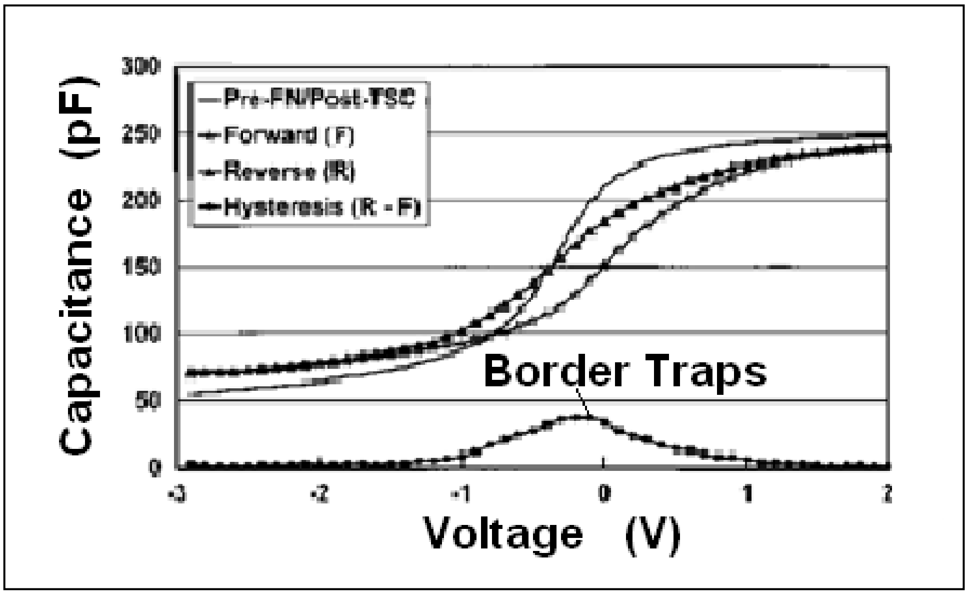

Fig. 1.23: *C–V hysteresis curves for 0.0013 cm2 n-substrate capacitors with a bias of 4 V. The asterisks are the C–V curves swept from accumulation to inversion; the triangles are the curves from inversion to accumulation, and the dots (lower peaked curve) are the difference in capacitance between the forward and reverse curves, that is, border traps. After Ref. [55]*

The effective border trap density, ΔN_{bt} is obtained by measuring *C-V* hysteresis and integrating the absolute value of the capacitance difference as [62-63]:

$$\Delta N_{bt} \approx (1/qA)\int \left|\left(C_{reverse} - C_{forward}\right)\right| dV, \qquad (1.31)$$

where, A is the capacitor area, q the elementary charge, $C_{reverse}$ refer to measurement from accumulation to inversion, and $C_{forward}$ refer from inversion to accumulation. Experimental data on border traps analysis are shown in Fig. 1.23.

1.9 Current conduction mechanisms in REOs dielectrics

In this section we discuss current conduction mechanisms in thin insulating films, in particular Rare-earth oxides (REOs) high-*κ* dielectrics. Several electrical conduction mechanisms are being accounted to explain the current conduction mechanisms in various high-*κ* dielectrics as are given in *Table 1.3.*

Table 1.3: *Basic conduction mechanisms and their temperature and voltage dependence characteristics, according to [8]*

Process	Expression	Temperature and Voltage Dependence
Schottky Emission	$J = A^* T^2 \exp\left[\frac{-q(\phi_B - \sqrt{qE/4\pi\varepsilon_i})}{kT}\right]$	$\sim T^2 \exp(+a\sqrt{V}/T - q\phi_B/kT)$
Frenkel-Poole Emission	$J \sim E \exp\left[\frac{-q(\phi_B - \sqrt{qE/\pi\varepsilon_i})}{kT}\right]$	$\sim V \exp(+2a\sqrt{V}/T - q\phi_B/kT)$
Tunnel or Field Emission	$J \sim E^2 \exp\left[-\frac{4\sqrt{2m^*}(q\phi_B)^{3/2}}{3q\hbar E}\right]$	$\sim V \exp(-b/V)$
Space-charge limited	$J = \frac{8\varepsilon_i \mu V^2}{9d^3}$	$\sim V^2$
Ohmic	$J \sim E \exp(-\Delta E_{ac}/kT)$	$\sim V \exp(-c/T)$
Ionic Conduction	$J \sim \frac{E}{T} \exp(-\Delta E_{ai}/kT)$	$\sim \frac{V}{T} \exp(-d'/T)$

Here, $a = \sqrt{q/(4\pi\varepsilon_i d)}$, A^* = effective Richardson constant, Φ_B = barrier height, E = electric field, ε_i = insulator dynamic permittivity, m^* = effective mass, d= insulator thickness, ΔE_{av} = activation energy of electrons, ΔE_{ai} = activation energy of ions. $V= E_d$. Positive constants independent of V or T are *b, c, and* d'.

In Ce, Dy, Gd of the REOs there are two dominating conductions mechanisms observed. For example, in Cerium oxide [64-65] the conduction mechanism at low field is Schottky emission (SE), while at higher field the conduction mechanism is Poole- Frenkle (P-F) mechanism.

The same has been observed for the Gd_2O_3 [66-67] high-κ dielectrics, that is, Schottky emission and Frenkle- Pool mechanism at low and higher filed respectively. Nevertheless, for Dy_2O_3, mainly bulk-limited [68] current conduction mechanisms have been reported [69], that is, at low field the space-charge-limited-current (SCLC), while at higher temperature Schottky emission has been observed.

1.10 Reliability Issues

1.10.1 Introduction

High- κ dielectrics have been known to be "trap-rich" materials. A number of efforts were carried out to improve high-κ dielectrics characteristics. For example, high temperature deuterium and forming gas anneals and O_3 surface treatments have been shown to reduce interface state [70]. The origin of the traps in high-k dielectrics, however, still remains a question. These pre-existing traps may play an important role in dielectric wear-out as well as device performance. In order to evaluate reliability, it is necessary to pinpoint the factors that influence the breakdowns of high-κ dielectrics (REOs), and their gate stacks (For example, REO/HfO_2). This work addresses reliability issues such as charge trapping and detrapping characteristics, stress-induced leakage current (SILC), dielectric breakdown, voltage dependent dielectric relaxation, Maxwell-Wagner current instabilities in the gate stacks, finally the combined effects of charge trapping, SILC, Maxwell-Wagner current instability and dielectric relaxation have been analyzed and discussed.

1.10.2 Reliability of MOS

Reliability of MOS devices is generally defined as [71]:

> *"The probability that the device will perform its required function under defined conditions for a specified period of time".*

In the specific case of a thin oxide thin the required function is to act as a sufficient insulator; the stated conditions are the stress voltages, currents and temperature that correspond to normal device operation; and the stated period of time is the required dc-lifetime of the product, which is usually taken to be 10 or 25 years, depending on the application.

1.11 Oxide defects charges

1.11.1 Classification of Oxide defects charges

The defects charges are basically classified with respect to their location and action as follows:

- **Interface-state charges Q_{it}**, which are located so close to the high-κ/ Ge interface and have energy states so close to E_F variation range of the semiconductor, that is, mainly within the Ge bandgap as to be able to exchange charges with the semiconductor in a short time.
- **Fixed oxide charges Q_f**, which are located at /or very near the interface but cannot exchange charges unlike Q_{it}.

- **Oxide-trapped charges, Q_{ot},** the trap sites of which are distributed inside the bulk of the oxide and capture (or emit) the charges brought into the dielectric film by hot-carrier injection, and so on.
- **Mobile ionic charges, Q_m,** such as sodium ions, which are mobile within the oxide under bias-temperature aging conditions. These charges are illustrated in the following Fig. 1.24.

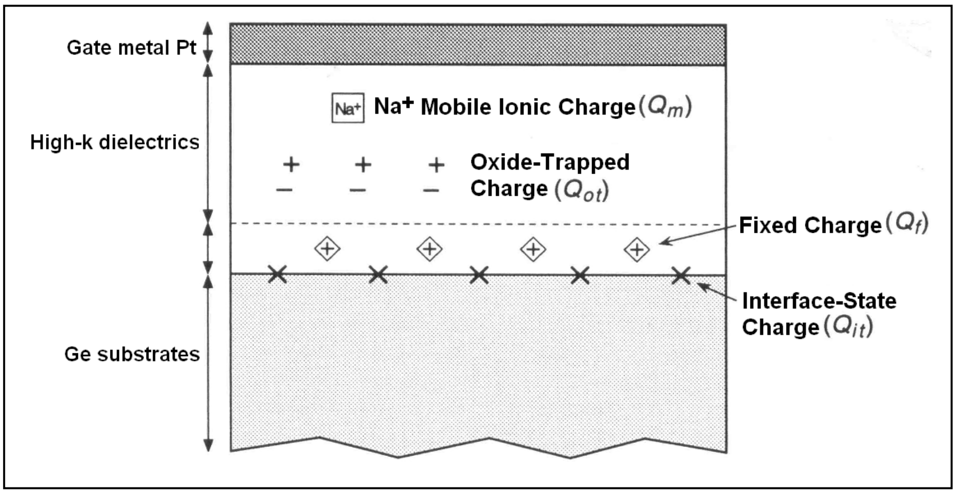
Gate metal Pt
High-k dielectrics
Ge substrates
Na+
Na+ Mobile Ionic Charge (Qm)
Oxide-Trapped Charge (Qot)
Fixed Charge (Qf)
Interface-State Charge (Qit)

Fig. 1.24: Terminology for charges associated in the MOS devices under bias condition.

1.11.2 Types of defects in MOS devices

Possible defect types and their impact on device performance are listed in the table 1.4. The specific problems caused by the defects include these: they initiate degradation; they cause charge trapping; and they create fixed charge, which cause carriers scatter in the semiconductor substrates.

Table 1.4: *Possible defect types and their impact on device performance. After Ref.[20]*

Origin of defects	**Defects type**	**Possible role**
Imprecise stoichiometry	Vacancies or interstitials, annealing induced	Fixed charge, SILC; motion under applied field.
Feature of polycrystallinity	Grain boundaries and associated defects, e.g. vacancies	Charge diffusion
Amorphous structure	Structure induced traps	Leakage current
Interface	Wrong bonds, relaxation with associated dipoles, roughness	Dipole, charge, electric field

1.12 Defects generation under electrical stress

The scaling of the SiO_2 gate layer thickness in advance generations of complementary-metal-oxide-semiconductor (COMS) processing is reaching its limit, both points of view of leakage current limitations as well as intrinsic reliability concern. By using a thicker gate insulating layer with a higher dielectric constant than SiO_2 (3.9), the leakage current flowing through the device is expected to decrease, and the reliability of the gate dielectric is expected to improve. However, defect generation in these high-κ materials under electrical stress, which is closely related to the reliability of the devices, has not yet been extensively studied. Defect build-up in these devices is investigated by monitoring the variations of the current density and the capacitance-voltage (*C-V*) characteristics of the structures during gate voltage stress experiments [72]. It is clear that defect generation is the key factor determining the oxide degradation and breakdown.

Three trap/defect generation models are illustrated in Fig.1.25, such as

(i) 'Anode hole injection model',

(ii) 'Hydrogen release model', and

(iii) 'Electric field energy model'

In the anode hole injection model [73], as illustrated in Fig. 1.25 (a), it is assumed that the holes tunneling back to the cathode can create electron traps in the oxide, probably in conjunction with an electron in the high-k dielectric conduction band. The physics of the trap creation process (Fig. 1.26) is still speculative. Indeed, there have been several studies demonstrating that the interaction of electrons and holes in an oxide results in trap creation [74]. However, the precise role of electrons and holes in the trap creation process and the details of the microscopic mechanism of the trap creation are still uncertain. The most important difficulty in studying this effect is the inability of many techniques to

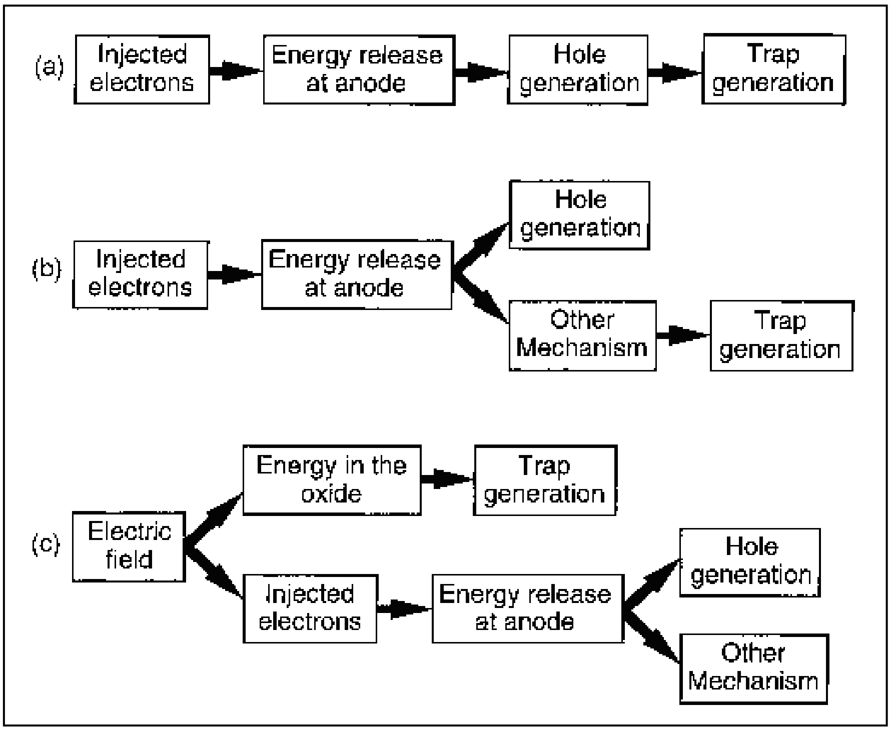
(a)
Injected electrons
Energy release at anode
Hole generation
Trap generation
(b)
Injected electrons
Energy release at anode
Hole generation
Other Mechanism
Trap generation
(c)
Electric field
Energy in the oxide
Trap generation
Injected electrons
Energy release at anode
Hole generation
Other Mechanism

Fig. 1.25: Outline of the three lines of thought on defect generation under stress that can found in literature. After Ref. [71]

separately control the hole and the electron injection. If there exists a voltage limit to anode hole injection, it could be questioned whether this model will correctly predict the low voltage oxide reliability.

The generation of interface defects, bulk defects, and positive charge under gate injection can be explained by the "Hydrogen release model" [75] is shown in Fig. 1.25(b). In the hydrogen release model (see Fig. 1.27), the electrons tunnel through the oxide potential arrier and reach the anode with sufficient energy to release hydrogen from the anode/oxide interface.

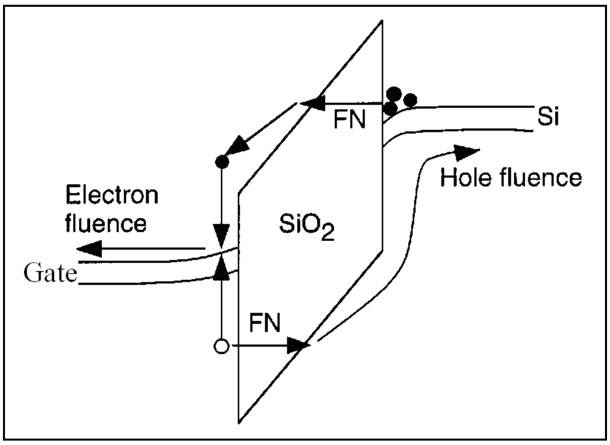

Fig. 1.26: *Schematic illustration of the anode hole injection model. Injected electrons reach the anode with high energy and can generate hot holes that can tunnel back to the cathode. After Ref. [71]*

This hydrogen is always present in sufficient amounts because of interface annealing applied to reduce the initial interface trap density. The released hydrogen diffuses through the oxide and can generate electron traps.

Some authors have even suggested a third possible route which is illustrated in Fig. 1.25(c). The electric field itself induces sufficient energy directly into the oxide to cause electron trap creation (electric field energy model). With this interpretation, all processes that are related to the energy release of the injected electrons at the Anode are independent of the trap generation mechanism.

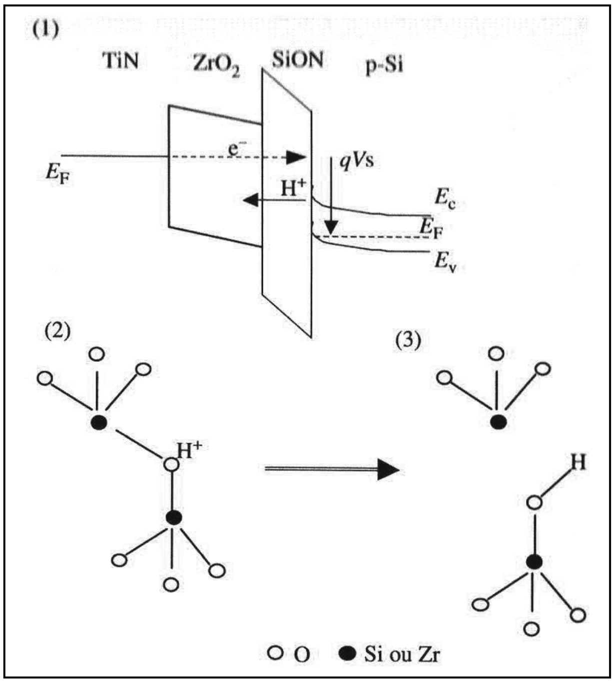

Fig. 1.27: *Schematic illustration of the hydrogen release modeling a TiN//ZrO_2/SiON/Si structure, stressed under gate injection. After Ref. [20]*

1.13 Dielectric Breakdown

1.13.1 Introduction:

The dielectric breakdown of the oxide layer in a MOS structure can be defined as a local increase of the system's conductance. This change can be abrupt or gradual depending fundamentally on the oxide thickness, device area, stress condition, and is often accompanied by a noisy behaviour [76]. Once broken down, in general, the MOS device will suffer from so much increased conduction across the gate dielectric film that it will no longer operate well, and cannot be recovered. The dielectric breakdown thus causes a fatal failure in integrated circuits, usually setting a major practical limit of mass production. One of the features most different from other MOS parameters is its statistical nature; that is, breakdown strength is not an average characteristic over the device area, but it is determined by the weakest defect spot across its surface.

1.13.2 Types of breakdown:

There are mainly two types of stress leading to dielectric breakdown, such as

a) Time-Zero Breakdown (TZBD)

b) Time-Dependent Dielectric Breakdown (TDDB)

a) Time-Zero Breakdown (TZBD): TZBD is accelerated by ramping up the applied voltage, usually until breakdown for every individual sample (Fig.1.28). TZBD is independent of stress time but depend on other parameters, for example, applied field across dielectric, the field at the breakdown is called field to breakdown, E_{BD}. A TZBD test requires a lot of (typically 50 to 100 or even more) samples devices due to the statistical nature of breakdown.

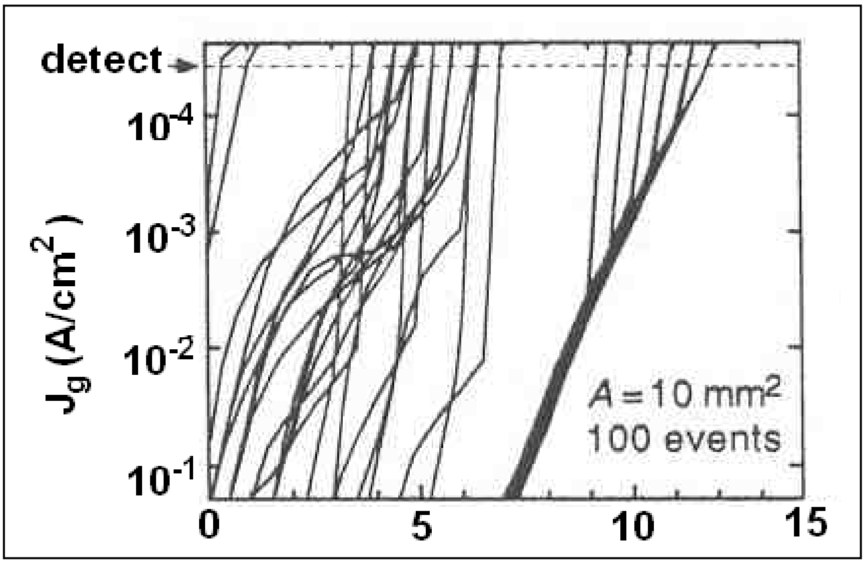

Fig. 1.28: Current density J_g vs. applied field E_{ox} for individual sample in ramp-voltage stress (RVS) breakdown. TZBD test. After Ref. [77]

b) Time-Dependent Dielectric Breakdown (TDDB):

TDDB is usually examined under constant voltage stress (CVS) and so requires a longer time. However, in general, TDDB has the merit of being more straightforward with respect to reliability, especially for non volatile memories. Another merit of TDDB is its capability to predict the breakdown life time t_{BD} and the failure rate at a certain operation voltage. From TDDB measurement one can charge-to-breakdown, Q_{BD}, that is, the totally injected electron charge until the device breakdown. Also from TDDB CVS measurement one can extract the total inject charge, Q_{inj} under bias.

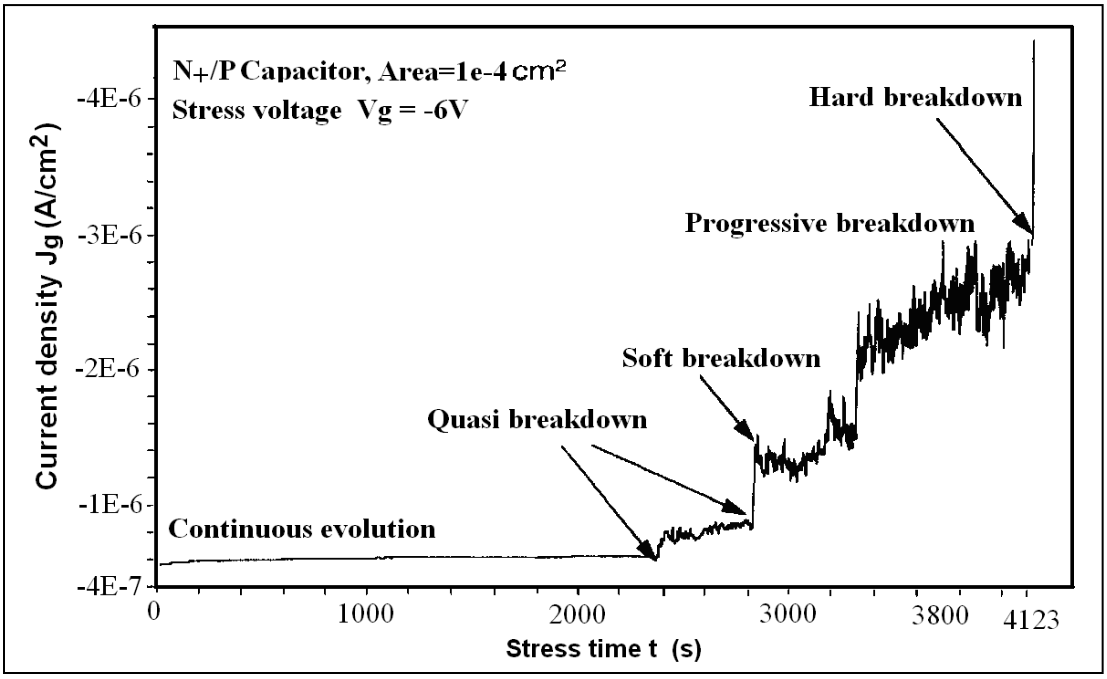

Fig. 1.29: *Current-time characteristics for a 4.5nm MOS gate oxide recorded during a CVS at 11.4 MV/cm. After Ref. [78].*

Time-Dependent Dielectric Breakdown (TDDB) is exemplified in the Fig. 1.31. It is interesting to note that during the TDDB measurement under the CVS condition there are several breakdown stages occurring in the device (Fig. 1.29). That is, in 1992, Fukuda and co-workers [79] presented experimental results showing that ultra-thin oxides exhibited a different breakdown, the associated current being orders of magnitude less than the tunneling current. This led to name the failure modes as stress-induced leakage current (SILC), quasi, soft breakdown (SBD) and progressive breakdown (PBD), identified with the low-conduction state, and the final, catastrophic or hard breakdown (HBD), identified with the high-conduction state. Fig. 1.30 shows typical *I–V* characteristics corresponding to SBD and HBD events.

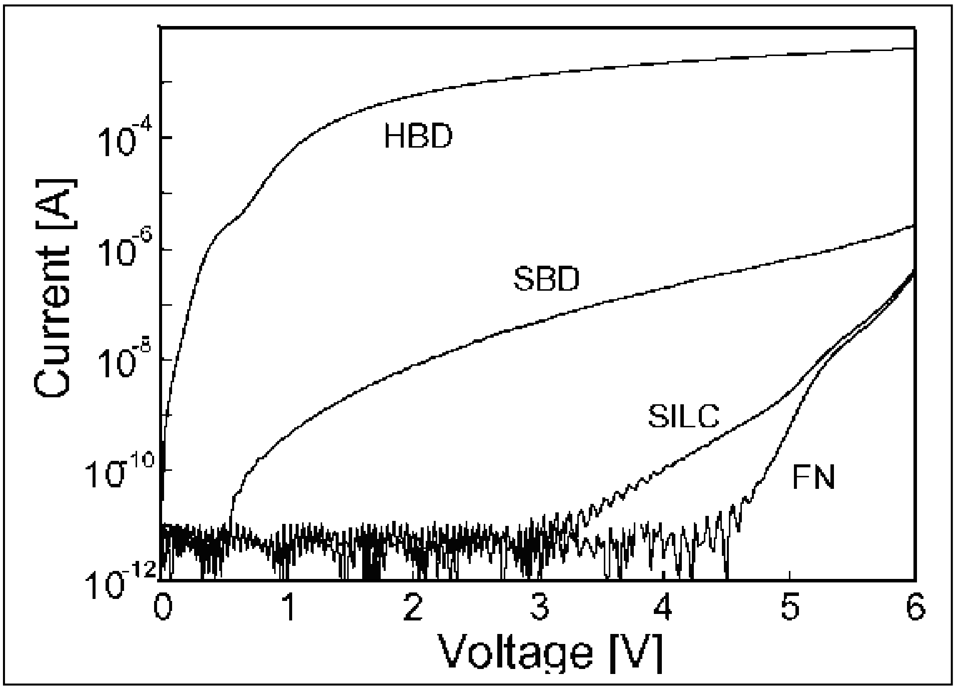

Fig. 1.30: *Current–voltage characteristics at different stages of oxide degradation. Fowler–Nordheim (FN), stress-inducedleakage- current (SILC), soft breakdown (SBD), and hard breakdown (HBD) curves are shown. Oxide thickness is 4.3 nm, device area is 6.4×* 10^{-5} *cm*^{2} *and p-type substrate. After Ref. [80]*

> *"The SBD can be defined as an oxide breakdown without the lateral propagation of the breakdown spot due to thermal damage [81]".*

> *"The HBD associated with and without significant thermal effects, i.e. with and without lateral propagation of the damage [82]. After SBD the Joule heating in the local conductive path leads to lateral propagation of the leakage spots and the oxide is finally broken down, signified as a hard breakdown (HBD) [83]".*

Although SBD has been mostly reported to occur in sub-5 nm oxides, some authors have claimed that thicker oxides may also exhibit this mode [84]. In practice, breakdown modes are often identified simply as SBD or HBD and since a physics-based sorting scheme is still lacking, the choice of whether a breakdown event belongs to one or another mode is at present rather ambiguous. Additionally, depending on the considered wear-out test, one or more breakdown events of either type can be induced in the same sample. Each jump of current in the characteristics is associated with the opening of a new breakdown spot across the oxide layer.

1.13.3 Percolation statistical breakdown model:

Beginning of the 1990s, Sune and co-authors [85] presented a `weakest link' breakdown model. It is assumed that during oxide stressing neutral electron traps are generated at random positions on the capacitor area, and the creation of critical amount of neutral traps causes capacitor breakdown [86]. It is assumed that electron traps are generated.

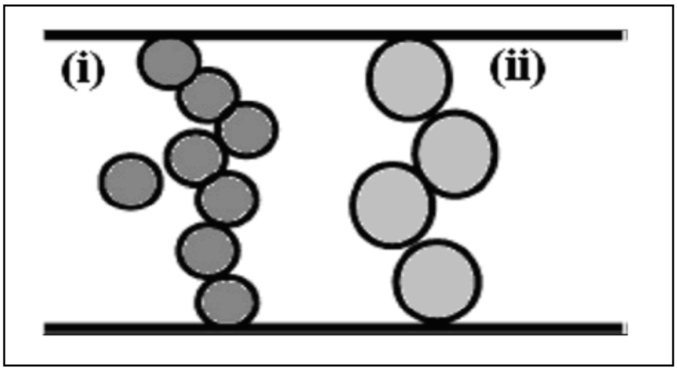

Fig. 1.31: A schematic presentation of the percolation theory of dielectric breakdown. It can be modeled as spheres that are randomly generated in the oxide during electrical stressing. When enough of these defects line up closely enough and span a dielectric film, breakdown occurs via conduction through this defect path. The bigger the defects are or the greater their sphere of influence (Fig 1.31 (ii)), the less defects it should take to produce a breakdown path. After Ref [87]

inside the oxide at random positions in space. If the two neighboring traps overlap (Fig.1.31 and 1.32), conduction path between these traps becomes possible. This mechanism of trap generation continues until a conducting path is created from one interface to the other, which is defining the breakdown condition, is defined as "Percolation statistical breakdown model" (Fig. 1.32).

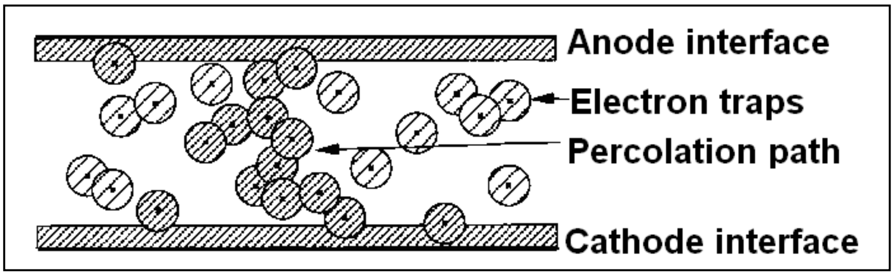

Fig. 1.32: *The percolation model for oxide breakdown explained step by step. As the density of neutral electron traps increases, conductive clusters of traps are formed ultimately leading to the creation of a conductive breakdown path from anode to cathode. After Ref. [19]*

1.14 Oxide Degradation

1.14.1 Introduction

The gradual degradation of the oxide properties during electrical stress, ultimately leading to breakdown, could happen in different ways, such as, (i) by means of light emission which is a localized effect [71], or (ii) the electrical degradation phenomena during stressing on the devices. First oxide breakdown was introduced by Harari [88] in 1978, a consensus has grown in literature that oxide degradation is the cause of the breakdown event in thin oxide layers. By degradation, we mean the continuous gradual deterioration of the oxide properties, which is a consequence of structural damage generated in the oxide. Several phenomena are related to dielectric degradation, for example, oxide charge trapping, i.e. negative and/or positive charge trapping; interface trap creation; creation of neutral electron traps and the generation of a stress-induced leakage current (SILC).

1.14.2 Oxide charge trapping characteristics

Charge trapping is a common phenomenon observed in most high-κ materials [89-97]. As a matter of fact, the use of dielectric layers with higher permittivity should allow us to use thicker films with equivalent electrical thickness than SiO_2, and one would expect to reduce charge trapping and the stress induced leakage current (SILC), thus improving the reliability of corresponding device. Trapping centers are not electrically active until they react with carriers bought into the oxide film by some stressing means. The charge-trapping behaviors may roughly be classified as negative charge trapping, positive charge trapping, as well as, interface-state generation. They are increasingly important from the reliability point of view as carrier injection is more likely to take place in today's MOS devices.

1.14.2.1 Negative charge trapping –detrapping characteristics

There have been lots of studies [8, 89-97] on negative charge traps mainly utilizing charge injection methods, and are frequently classified as in terms of the capture cross-section σ [98-99]. Most of all kinds, particularly, the small values for the capture cross section, like, 10^{-16} to 10^{-19} cm^2 suggest that the traps generated during the electrical stress are neutral centers. [98-100].

Charge trapping and detrapping could be studied by measuring flatband voltage shift (V_{FB}) of high-frequency (e.g 100kHz ~1MHz) capacitance–voltage (C–V) curves as a function of charging or discharging time (Fig.1.35) by using a pulsing technique also known as “Stress and sense technique” [101-102], which is briefly described in § 2.5.6. Usually fresh devices are used for each measurement. During charging, devices are stressed at the applied gate bias voltage in accumulation, that is, charges (electrons) are injected from substrate (for *n*-type) under constant voltage stress (CVS) conditions.

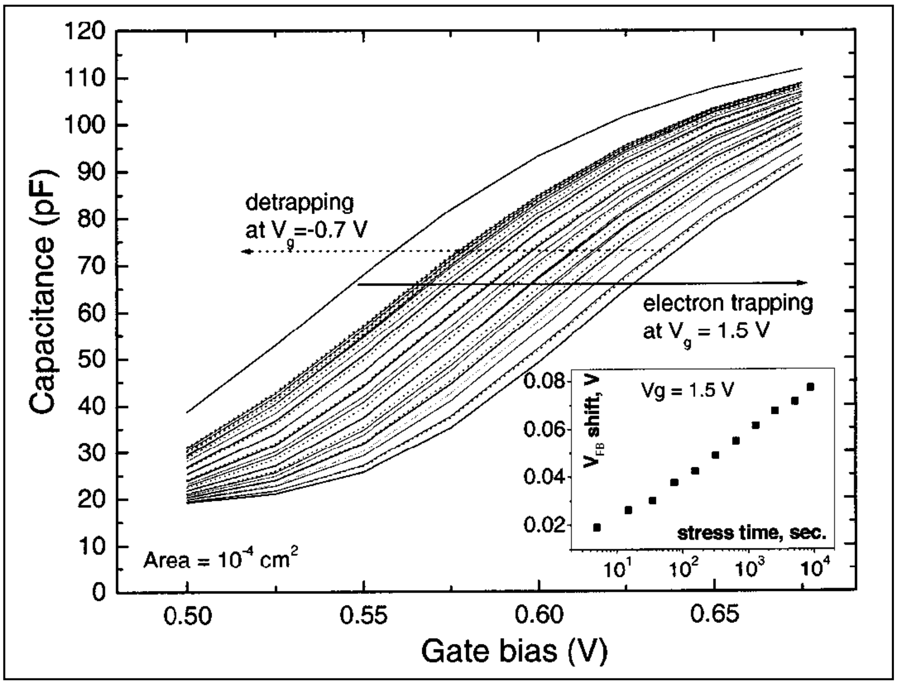

Fig. 1.33: *C–V characteristics taken between pulses of positive gate bias of 1.5V (solid lines) and during detrapping at Vg=-0.7V (dotted lines) at room temperature. The arrows indicate directions of flatband voltage shift over time during stress (solid arrow) and discharging (dotted arrow). Flatband voltage shift deduced from the C–V curves during charge trapping is shown in the inset as a function of stress time, charging time was 9000s while discharging time was 10000s. One can see* V_{FB} *shift during trapping follows power law dependence. After Ref. [103]*

During the injection of charges some the electron are trapped in the bulk of the oxides, and thus causing flatband voltage shift (V_{FB}), which is illustrated in Fig. 1.33 Immediately following charging, the gate voltage is reversed and the discharging or relaxation of shifted V_{FB} towards its original position was monitored as a function of time (see Fig. 1.33).

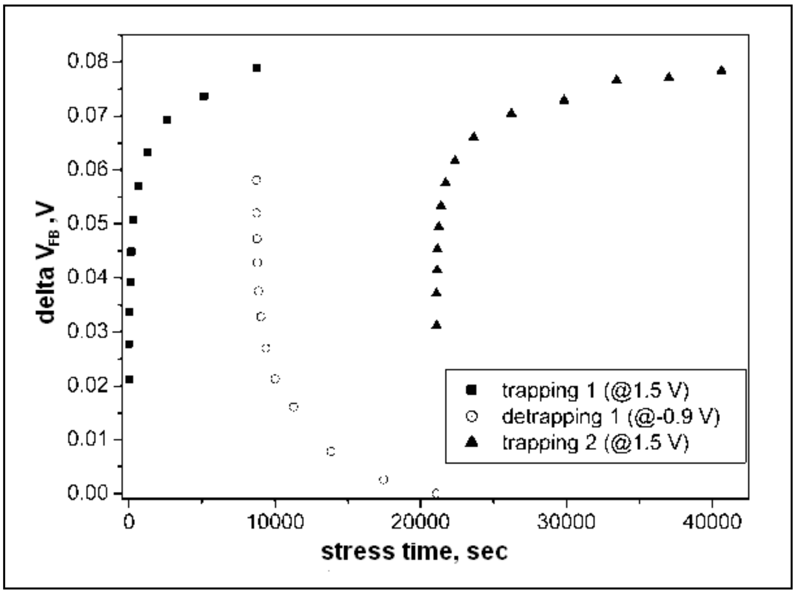

Fig. 1.34: *Kinetics of charging (at 1.5 V), discharging (at -0.9 V) and 2nd charging (again at 1.5 V). After Ref. [104]*

From trapping-detrapping (i.e. charging-discharging) measurement one can investigate how stable the trapped electrons are. One of the reasons for performing this set of discharging experiments is to better understand the nature of the trapping sites in high-k stacks. From V_{FB} vs. injected charge (Q_{inj}) curve one can easily estimate the total amount of trapped charges ($Q_{ot}=-\Delta V_{FB}C_{ox}$). Trapped charges at deep levels in the forbidden gap–shows a relatively slow discharging relaxation over time and Fig. 1.34 gives an immense clear picture of the level of trapped charges from "trapping-detrapping" measurements.

In (40-80nm) ZrO_2/Si (100) based MOS devices, Chavez, *et at.* [105] observes that a positive stressing results in a positive flatband voltage shift whereas negative CVS bias results in a negative shift. It is clear that a positive charge density results in a negative flatband voltage shift while the inverse is true for negative charge, that is, negative bias induces positive charge in the oxide (Fig.1.35).

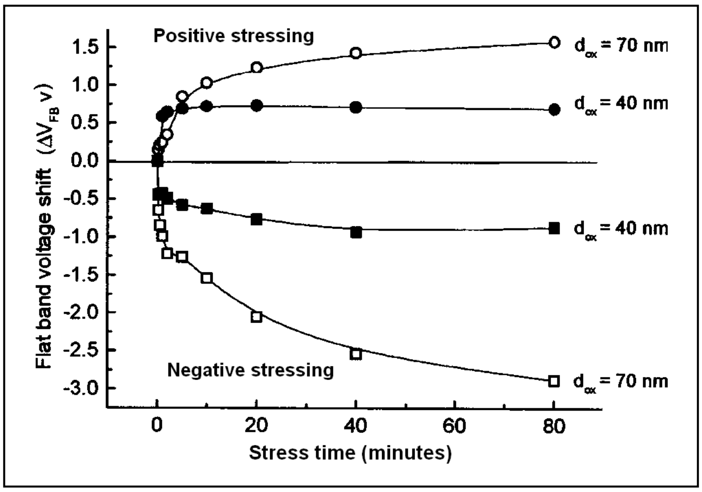

Fig. 1.35: *Flatband voltage shift as a function of stress time for 40 and 0 nm thick* ZrO_2 *films subjected to positive and negative 1 MV* cm^{-1} *electric fields. Cycling of the effect was observed by applying first one sense of stress then applying the opposite sign and magnitude of stress. After Ref. [116]*

With the objective of predicting V_{FB} shifts as a function of stressing time and injected charge density and gaining insights into the trapping physics, a model for charge trapping is developed for high-κ gate dielectrics. The model assumes that the total trap density (filled and empty) in the gate dielectric stack remains constant with stressing and that the stress induced flatband voltage shifts are mainly due to the trapping of electrons in existing traps; creation of additional new traps during stressing is assumed to be negligible. Flatband voltage shift V_{FB} as a function of stress time or injected charges can be express low field by an empirical power law, as [113-114, 106-107]

$$V_{FB} = V_{FB\max} Q_{inj}^{\alpha}, \tag{1.32}$$

where, V_{FBmax} the maximum flatband (V_{FB}), shift is a constant , Q_{inj} is the injected charge, and α is exponential power. The power law model (1.32) fit is shown is the Fig. 1.36.

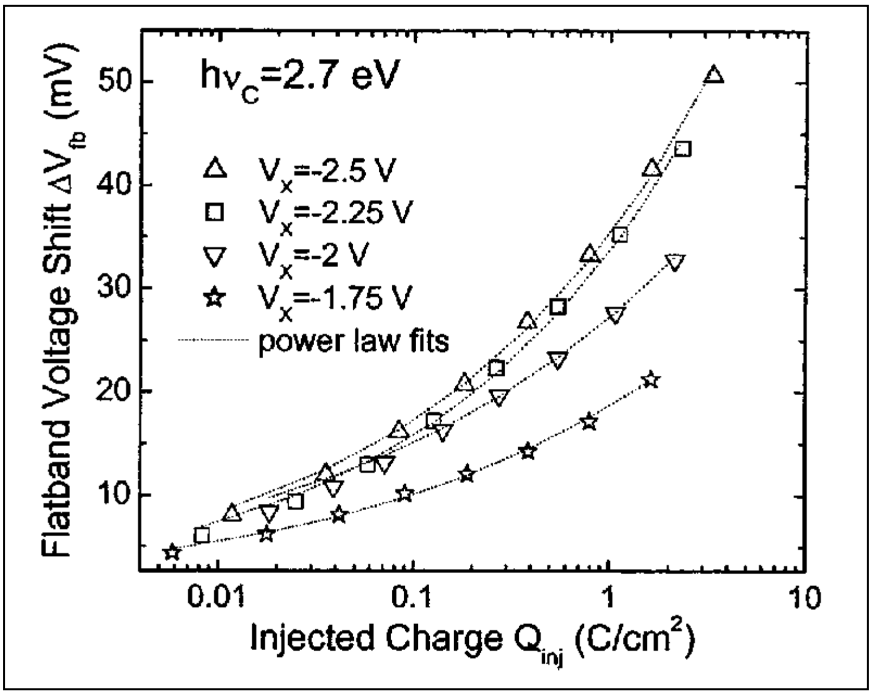

Fig. 1.36: *Flatband voltage shift in Al_2O_3 nFETs at different substrate biases and the same maximum photon energy $h\nu = 2.7eV$. Suppression of charge trapping occurs through reducing the substrate bias, in the figure the dotted line is the fit of Eq. (1.32) to experimental date. After Ref. [106]*

However, at higher filed the V_{FB} can be expressed as a function of total injected charge (Q_{inj}) [101-102]:

$$\Delta V_{FB} = \Delta V_{\max}\left\{1 - \exp\left[-\left(\frac{\sigma Q_{inj}}{q}\right)^{\beta}\right]\right\}, \tag{1.33}$$

where σ the neutral trap cross section, β is characteristics constant, that is, a measure of the distribution traps width, $\beta=1$ corresponding to a single value of charge trapping cross section with no continuous distribution in trap's value, while other terms are described above. Experimental data are fitted by charge trapping model with Eq. (1.33), shown in Fig .1.37.

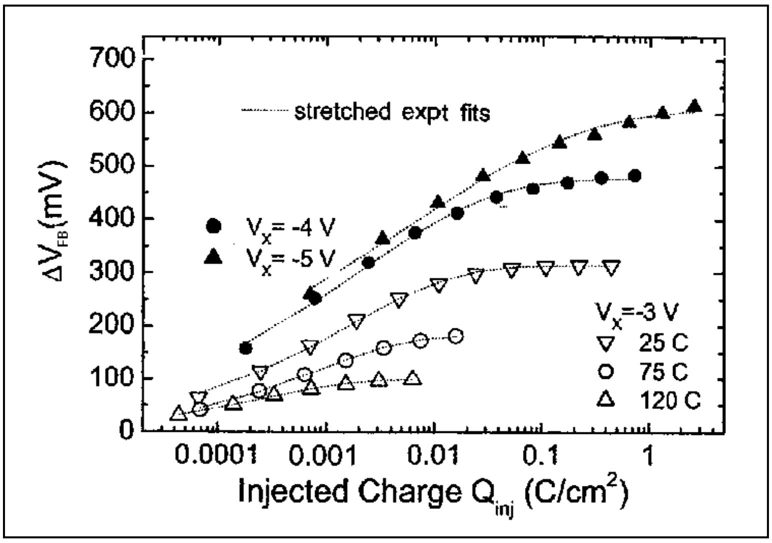

Fig. 1.37: *Temperature dependence of charge trapping as function of in HfO$_2$ n-FETs under different CVS conditions is shown in the figure. The injected charge is increased can be fitted to charge trapping model and the solid line (Fig. 1.37) the fit of Eq. (1.33) on experimental data. After Ref. [106]*

1.14.2.2 Positive charge trapping characteristics

According to the previous section, positive and negative flatband voltage shifts (ΔV_{FB}) are the indication of negative charge trapping (electron trapping) and positive charge trapping respectively (see Fig. 1.35). If the flatband voltage shift (V_{FB}) is negative under negative CVS on *p*-type MOS capacitor (at high frequency), that is, *C-V* shift at flatband toward negative voltage direction with progress of stress time, and it is an indication of positive charge trapping (Fig.1.38) [108]. This charge trapping will increase with the stress voltage increases (Fig. 1.39) [109].

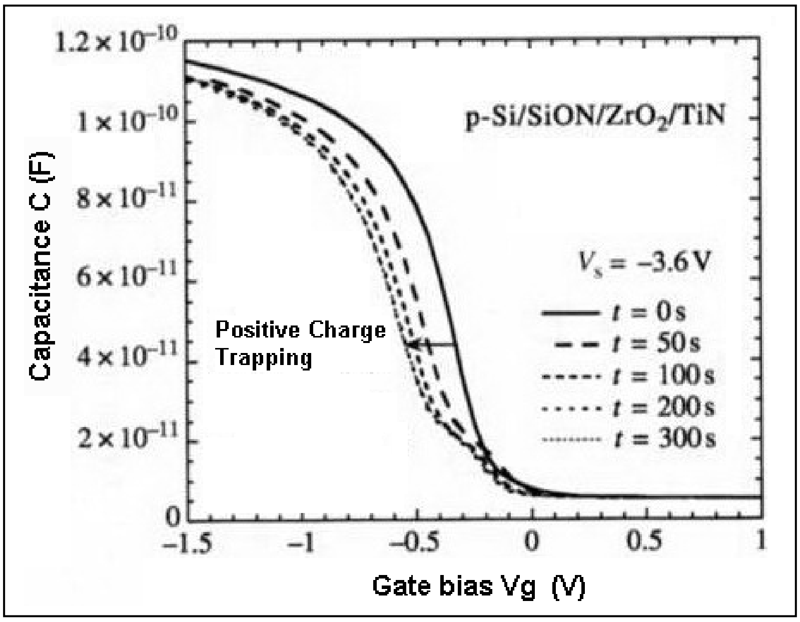

***Fig. 1.38**: C–V characteristics of p-Si/SiON/ZrO$_2$/TiN capacitors measured after different times of constant voltage stress at -3.6 V. The negative C-V shift is the indication of positive charge trapping in the capacitor during CVS. After Ref. [109]*

Two models are currently under debate to explain the generation of positive charge and neutral defects in ultrathin high-κ dielectric layers. In one model (the so-called "Anode hole injection model" (see § 1.12), one assumes that electrons arriving at the anode with sufficient energy can generate a hole by impact ionization, and this hole might tunnel back in the high-κ layer towards the cathode, creating defects in the high-κ layer [110-111].

The alternative model (the so-called "Hydrogen release model" (see § 1.12) assumes that electrons arriving at the anode with sufficient energy can release hydrogen (atomic or proton). This hydrogen species is then transported towards the cathode and can be trapped at oxide networks, leading to the generation of hydrogen-induced positive charge and neutral traps [108, 112-113].

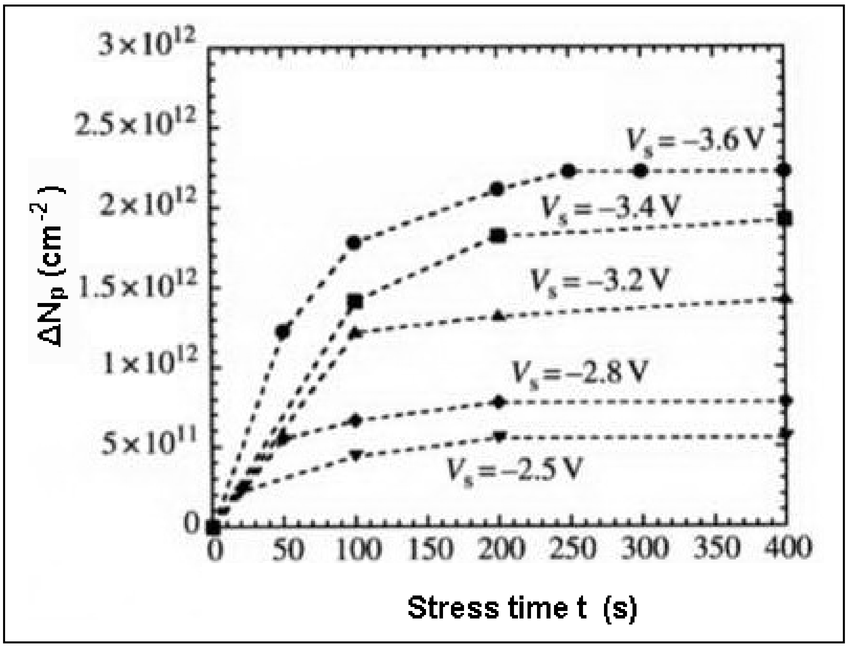

Fig. 1.39: *The time dependence of the density of a positive charge at different stress voltages as calculated from the shift of the C–V characteristics of the TiN/*ZrO_2*/SiON/p-Si capacitors, where* ΔN_p *is the total positive traps density during constant voltage stress. After Ref. [109]*

1.14.3 Stress-induced leakage current (SILC) and neutral traps

Generally, two types of traps are associated with the leakage current of the oxide layer: interface-trapped charge and oxide-trapped charge. The interface-trapped charges originate from defects such as structural defects related to the deposition process, metallic impurities or bond-breaking process at the insulator–substrate interface. However, oxide-trapped charges are associated with defects in the high-k dielectric materials (e.g. CeO_2, Dy_2O_3, HfO_2), are found to depend mostly on the injecting electrode. Under CVS as time progresses, applied voltage generates traps in the oxide [19]. These traps act both as coulombic scattering centers and as pathways for increased, local leakage currents, usually called SILC [114]. The traps that are generated during a high voltage stress are charged negatively near the cathode [19] and positively near the anode due to electrons tunneling into and out of the traps. The measured total current density (J_{mea}) at any time (t) and at a fixed voltage is a sum of three different components:

$$J_{mea} = J_{tun} + J_{leak} + J_{SILC}(t), \tag{1.34}$$

where, J_{tun} is the tunneling current in an ideal oxide having no traps. $J_{leak}(0)$ is the leakage current due to neutral electron traps that exist in fabricated devices and $J_{SILC}(t)$ is the SILC contribution. Some researchers have proposed that SILC is caused by interface-state generation [115], while others claim that it is due to bulk-oxide electron-trap generation [116]. Another possibility for the origin of the SILC is the generation of the neutral oxide trap in the bulk high-k , since the trap sites behave as neutral centers in the absence of bias, but behave as acceptor-like and/or donor-like trap centers during electrical biasing [117]. Still others have proposed that it is due to non-uniformities or weak spot formations in the oxide films [118]. SILC can be measured from the difference of the pre-stress gate current [J_0 (fresh)] and post-stress gate current [J_g (stress)], i.e.

$$J_{SILC} = [J_g(stress)] - [J_0(fresh)], \tag{1.35}$$

It is observed that the magnitude of gate leakage current is increased with increasing the applied stressing time (Fig. 1.40), which signifies that the larger stressing time generates more neutral traps, and more electrons tunnel from cathode to traps and traps to anode mostly inside the oxide. SILC is composed of two components: a transient component and a DC component [119]. The transient component consists of trap filling, as electrons transport from cathode into traps too distant from the anode for efficient tunneling to the anode. The trap-assisted tunneling or Poole-Frenkel emission through the oxide causes the DC component. Stress-induced leakage current (SILC) is now the limiting factor for down scaling the tunnel oxide thickness in

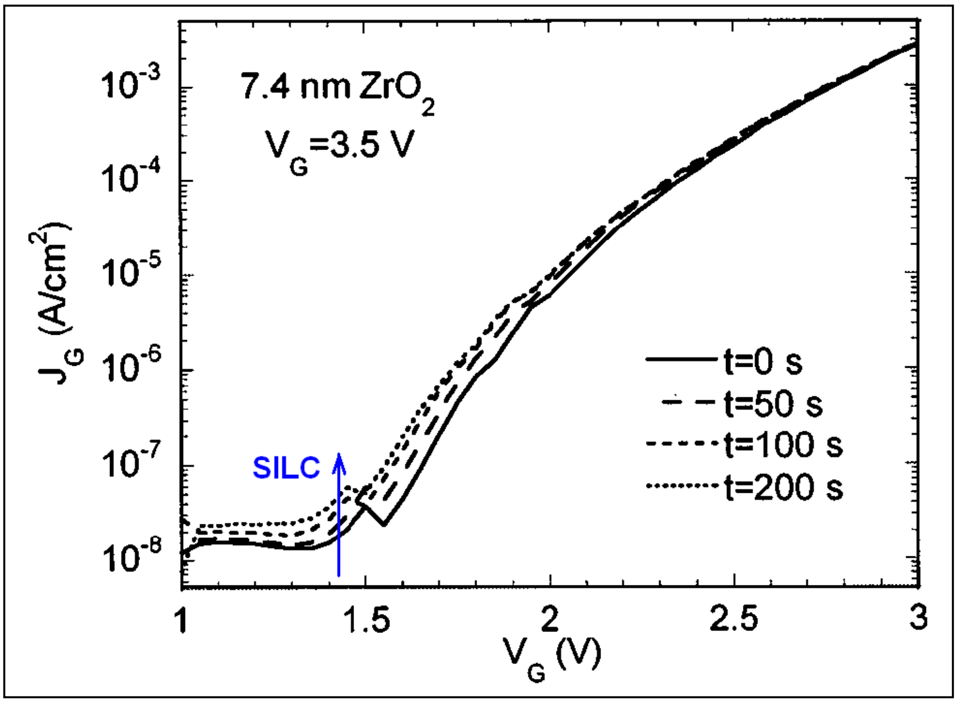

Fig. 1.40: *Current(J_G)–voltage(V_G) characteristics of a MOS capacitor with a 7.4 nm ZrO2 layer recorded after different times of constant gate voltage stress at 3.5 V. The $J_g(t)$-J_0 (0) is the measure of stress-induced leakage current (SILC). After Ref. [120].*

complementary-metal-oxide-semiconductor (CMOS) (Si-based). SILC through the gate dielectric of a MOS transistor causes an additional power consumption which is unwanted especially in low power applications; there it may become a reliability issue in those deep-submicron technologies where SILC dominates over the direct- tunneling or leakage current [121].

It has been widely accepted that SILC path is very localized and measurements on large capacitors can reproducibly reveal the average current density, while a kind of random telegraph signal can be observed on very small capacitors [122]. It was clear since the beginning of this decade that SILC is partially due to a transient

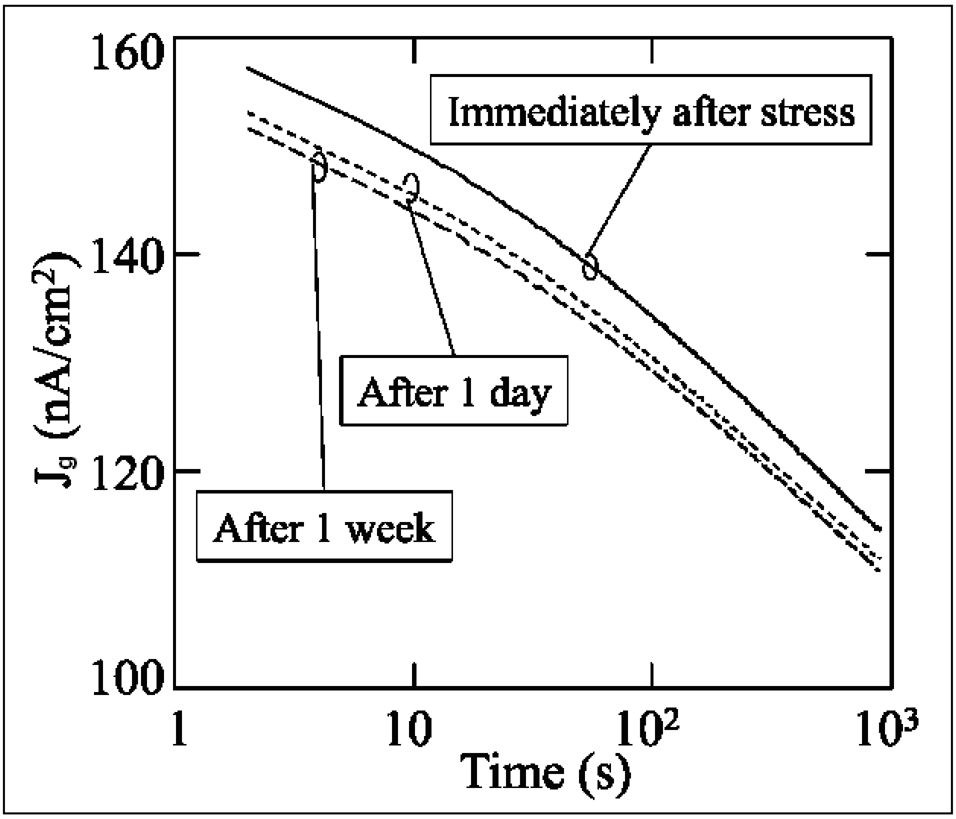

Fig. 1.41: *SILC decay (at Vg=4.7V and Eox=6.7) as function of time. Different time elapsed between constant voltage stress (CVS) and measurements. After Ref. [125].*

contribution, which decays with times [123], and also this time-decay behavior could be interpreted as the physical mechanism of charge trapping-detrapping from oxide defects[124]. Cester, *et. al.* [125] explained the time-decay SILC (see Fig. 1.43) by two mechanisms, such as, one is local relaxation of lattice, while other is weak spot clogging by injected electrons. It is widely accepted that the origin of the SILC is the generation of the neutral oxide traps in the bulk of high- κ gate dielectrics [117], when the local trap density reach a critical value, a chain of traps is formed across the oxides, at this time, the current flow become localized and breakdown occurs [19].

1.15.1 Maxwell-Wagner Instability

Charge trapping at the interface between the two dielectric layers of a high-*κ* gate stack is shown to be caused by "Maxwell-Wagner-Instability". The fact that the two layers of a high-*κ* gate stack have different compositions means that they will also have different conductivities [126]. Then, the application of a gate bias will immediately produce a discontinuity in current density at the interface between the two layers, causing charge to accumulate there until, in steady state, the same current density flows through both layers. If the gate bias is removed, a discontinuity in current density will again be produced, this time causing the charge to rush out of the gate stack, as the experiments described above seem to suggest.

This behavior has not previously been discussed a lot in the literature on high-*k* gate stacks. However, it is a well-known and ancient phenomenon, having first been described in the 19th century by Maxwell himself [127], then somewhat later and more extensively by Wagner [128]. Together these two effects are called "Maxwell–Wagner polarization," As they produce electrical instabilities in MOS devices, it could be refer as "Maxwell–Wagner instability" to emphasize its time-dependent nature. However, Maxwell–Wagner instability is not the only electrical instability known to exist in high-*k* gate stacks; a second is dielectric relaxation of the high-*k* layer.

1.15.2 Dielectric relaxation

The effect of dielectric relaxation can influence the performance of MOS devices with high-gate oxide, such as the drive current variation and high frequency properties. Dielectric relaxation is a bulk-related phenomenon, which causes relaxation current following the direction of *dV/dt*. Reisinger *et al.*, and Jameson *et al.*, attributed the observed current transients to dielectric material polarization relaxation [129-130] induced by carrier hopping in double potential well. In a recent publication, X. Zu, *et al.* [131] explained the dielectric relaxation current by electron trapping and detrapping in the high-κ dielectrics. It has been detected in polycrystalline, disordered, or amorphous films but not in single-crystal dielectrics [132].

Dielectric relaxation is a well-known and ancient phenomenon, having also been discovered in the 19th century by Curie [133], and then rediscovered later by von Schweidler [134].

$$J_e / P = \alpha t^{-n}, \tag{1.36}$$

where J_e is the relaxation current density (A/cm^2), P is the total polarization or surface charge density (V nF/cm^2), α is a constant in seconds and n is a real number close to 1. This is now referred to as the “Curie–von Schweidler law” [135].

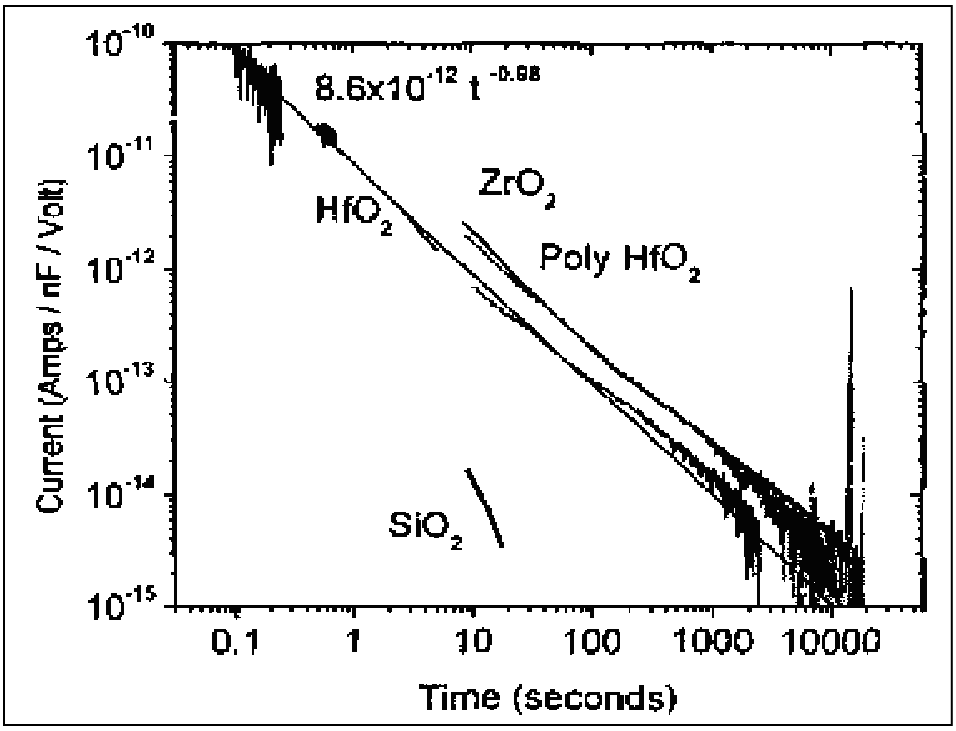

Fig. 1.42: Dielectric Relaxation currents for SiO_2, ZrO_2, and amorphous and polycrystalline HfO_2. The current is scaled by capacitor size (nF) and applied bias (V). Breaks in the amorphous HfO_2 data are due to the electrometer switching current ranges. A fit of $1/t^n$ *to the amorphous HfO_2 data is also shown. After Ref. [9]*

It is often studied by measuring the transient current that flows in an RC circuit, seems to universally have a time dependence of $1/t^n$, with n slightly less than 1. This time dependence has been observed in materials such as SiO_2, Si_3N_4, Al_2O_3, ZrO_2, HfO_2, Ta_2O_5, Y_2O_3, perovskites and others. In particular, dielectric relaxation is often the dominant contribution to the dielectric loss of perovskite thin films, making it widely studied in connection with DRAM technology [130]. Because dielectric film has very low conductivity, this is a slow process in which the relaxation current decays with time following the Curie–von Schweidler law [135]. The physical nature of dielectric relaxation can be explained with the potential well model in terms of dipole orientation [130]. Dipoles, which are homogeneously distributed inside a material, are formed by localized defects and disorder due to a lack of crystallinity. The orientation is formed as charge carriers hop over potential barriers under the influence of an electric field. However, this charge transfer is confined to a relatively few neighboring sites.

The direction of the leakage current and relaxation current depend on the polarities of V and dV respectively, can have the same or opposite directions. The directions of these two currents on high-k dielectric stressed in the accumulation region with a bias changing from a negative voltage to zero are illustrated in Fig. 1.43. Under this stress condition and our measurement setting, the leakage current is negative and the relaxation current is positive.

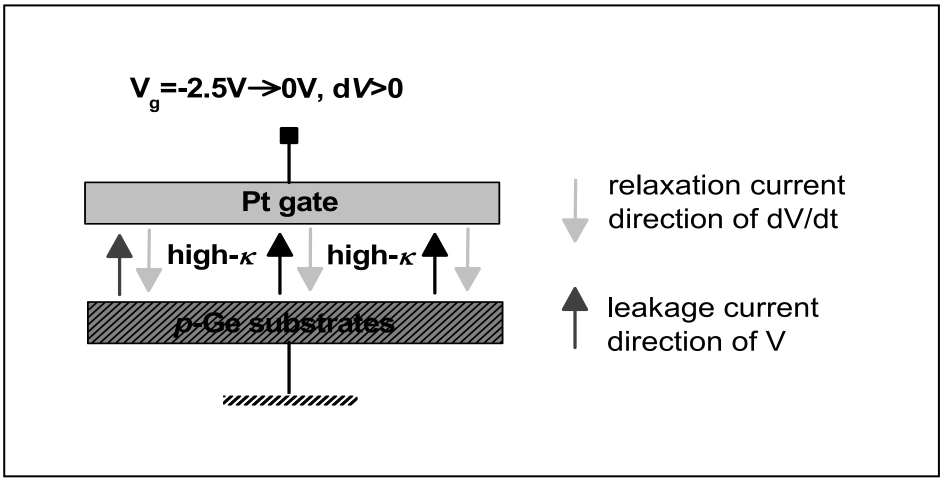
V_g=-2.5V→0V, dV>0
Pt gate
high-κ
high-κ
p-Ge substrates
relaxation current direction of dV/dt
leakage current direction of V

Fig. 1.43: Schematic diagram of the leakage current and relaxation current in high-k gate dielectric with changing bias V_g.

Maxwell–Wagner instability is shown to be coupled to a second instability, dielectric relaxation of the high-κ layer; continuity of current in steady state requires that the electric fields in the two dielectric layers remain fixed, so the change in polarization of the high-*k* layer due to dielectric relaxation must be compensated for by the conduction of additional charge to the interface. Evidence for this behavior in high-*k* gate stacks is found in the thickness dependence of their dielectric relaxation current, with the correct dependence being obtained only from a model in which the two instabilities act simultaneously. If the two dielectrics (in gate stacks) are perfectly insulators, this filed will be $V_{appl} k_2 /(d_1 k_2 + d_2 k_1)$, where the dielectric constants of layer 1 and 2 will be simply $k_1 = 1 + \chi_1$ and $k_2 = 1 + \chi_2$, χ_1 and χ_2 being the dielectric susceptibilities, d_1 and d_2 the thickness of the bi-layers 1 and 2 respectively, then the relaxation current due to these effects can be express as [136]:

$$J_g = \frac{2V\kappa_2\sigma_{0,1}}{d_1\kappa_2 + d_2\kappa_1}\left(3 + \ln\frac{t}{t_{0,1}}\right)\frac{t_{0,1}}{t}, \quad t > t_{0,1}. \tag{1.37}$$

where $\sigma_{0,1}$ and $t_{0,1}$ are the material constants which set the scale of current and time respectively, other terms are defined above. Uniform dielectrics do not exhibit Maxwell–Wagner instability, and perfect crystals do not exhibit dielectric relaxation, making the ideal high-*k* gate dielectric a uniform single-layer perfect crystal bonded epitaxially to the semiconductor (e.g. Si, Ge) substrates. In Dy_2O_3/HfO_2 gate stacks we studied and hence observed the above described “Maxwell-Wagner Instability” will be shown the results in chapter 6.

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Chapter 2

2. Experimental Details and Characterization Methodologies

2.1 Introduction

In the present work, the metal-oxide-semiconductor (MOS) capacitors were deposited by Molecular Beam Exitaxy (MBE). The reliability characteristic issues, such as, charge trapping, stress-induced leakage current (SILC), dielectric breakdown phenomena (DB), dielectric relaxation (DR) and electrical characteristics of Ge-based MOS devices where REOs as gate dielectrics were studied in the present thesis. Short descriptions of the above mentioned deposition technique (also other techniques those are being implemented in the CMOS technology), as well as extraction methodologies of reliability characteristics are illustrated in this chapter.

2.2 Various deposition techniques:

Amorphous high-*k* oxides are mainly deposited on semiconductors by atomic layer deposition (ALD) and metal organic chemical vapor deposition (MOCVD). These methods are compatible with semiconductor manufacturing offering very good uniformity and high throughput. Physical vapor deposition (PVD) methods, including molecular beam epitaxy/deposition (MBE/MBD) offer alternative possibilities. A short description of different deposition techniques are a stated below:

2.2.1 Chemical vapor deposition (CVD):

CVD is a chemical process used to produce high-purity, high-performance solid materials. The process is often used in the semiconductor industry to produce thin films. In a typical CVD process, the wafer (substrate) is exposed to one or more volatile precursors, which react and/or decompose on the substrate surface to produce the desired deposit. Frequently, volatile by-products are also produced, which are removed by gas flow through the reaction chamber.

Micro-fabrication processes widely use CVD to deposit materials in various forms, including: monocrystalline, polycrystalline, amorphous, and epitaxial. These materials include: silicon, carbon fiber, carbon nanofibers, filaments, carbon nanotubes, SiO_2, silicon-germanium, tungsten, silicon carbide, silicon nitride, silicon oxynitride, titanium nitride, and various high-k dielectrics. The CVD process is also used to produce synthetic diamonds.

2.2.2 Atomic layer deposition (ALD):

ALD is a thin film deposition technique that is based on the sequential use of a gas phase chemical process. The majority of ALD reactions use two chemicals, typically called precursors. These precursors react with a surface one-at-a-time in a sequential manner. By exposing the precursors to the growth surface repeatedly, a thin film is deposited.

ALD is a self-limiting (the amount of film material deposited in each reaction cycle is constant), sequential surface chemistry that deposits conformal thin-films of materials onto substrates of varying compositions. ALD is similar in chemistry to chemical vapor deposition (CVD), except that the ALD reaction breaks the CVD reaction into two half-reactions, keeping the precursor materials separate during the reaction. Due to the characteristics of self-limiting and surface reactions, ALD film growth makes atomic scale deposition control possible. By keeping the precursors separate throughout the coating process, atomic layer control of film growth can be obtained as fine as ~0.1 Å (10 pm) per monolayer.

2.2.3 Physical vapor deposition (PVD):

PVD is a variety of vacuum deposition and is a general term used to describe any of a variety of methods to deposit thin films by the condensation of a vaporized form of the material onto various surfaces (e.g., onto semiconductor wafers). The coating method involves purely physical processes such as high temperature vacuum evaporation or plasma sputter bombardment rather than involving a chemical reaction at the surface to be coated as in chemical vapor deposition. PVD is used in the manufacture of items including semiconductor devices, coated cutting tools for metalworking.

2.2.4 Molecular Beam Epitaxy (MBE):

MBE is one of several methods of depositing single crystals. It was invented in the late 1960s at Bell Telephone Laboratories by J. R. Arthur and Alfred Y. Cho. Molecular beam epitaxy takes place in high vacuum or ultra high vacuum (10^{-8} Pa). The most important aspect of MBE is the slow deposition rate (typically less than 1000 nm per hour), which allows the films to grow epitaxially. The slow deposition rates require proportionally better vacuum to achieve the same impurity levels as other deposition techniques.

During operation, RHEED (Reflection High Energy Electron Diffraction) is often used for monitoring the growth of the crystal layers. A computer controls shutters in front of each furnace, allowing precise control of the thickness of each layer, down to a single layer of atoms. Intricate structures of layers of different materials may be fabricated this way. Such control has allowed the development of structures where the electrons can be confined in space, giving quantum wells or even quantum dots. Such layers are now a critical part of many modern semiconductor devices, including semiconductor lasers and light-emitting diodes.

In systems where the substrate needs to be cooled, the ultra-high vacuum environment within the growth chamber is maintained by a system of cryopumps, and cryopanels, chilled using liquid nitrogen or cold nitrogen gas to a temperature close to 77 kelvins (-196^0C). Cryogenic temperatures act as a sink for impurities in the vacuum, so vacuum levels need to be several orders of magnitude better to deposit films under these conditions. In other systems, the wafers on which the crystals are grown may be mounted on a rotating platter which can be heated to several hundred degrees Celsius during operation.

Molecular beam epitaxy is also used for the deposition of some types of organic semiconductors. In this case, molecules, rather than atoms, are evaporated and deposited onto the wafer. Other variations include gas-source MBE, which resembles chemical vapor deposition.

2.2.4.1 Advantages of MBE deposition technique:

MBE processes various advantages of over other deposition techniques (e.g. CVD, ALD) during the deposition gate dielectrics on semiconductor substrates.

First, the native oxides of Si and Ge surfaces can be removed *in-situ* by thermal desorption under ultra high vacuum (UHV) conditions.

Second, because there is no need to develop precursor chemistry, a large number of high-κ candidates can be screened in a short time.

Third, MBE offers a wide temperature window for growth, including room temperature, which is not easily accessible by CVD-based techniques.

Finally, MBE offers the possibility of epitaxial growth of oxides to improve their dielectric properties (i.e., the dielectric permittivity-κ) and enhance their performance as gate dielectrics [1-3].

Other advantage of the MBE/MBD technique is that the oxides can be prepared using a wide temperature window which includes room temperature, not readily available by CVD-based techniques. The deposition temperature in many cases affects the interface quality, the microstructure, the density and the electrical quality of the films. Therefore, MBE is an excellent tool to optimize the quality of the dielectric [4]. In addition, according to the evidence we have so far, the MBE/MBD films directly deposited on a clean semiconductor surface present excellent nucleation, producing smooth continuous films. Nevertheless, MBE offers the possibility of epitaxial growth of oxides combined with epitaxial semiconductor overgrowth, which could lead to integration of heterogeneous metal oxide/semiconductor device structures such as fully epitaxial semiconductor-on-insulator or resonant tunneling structures. In the present work Ce, Dy, La, and Hf are evaporated from an e-beam evaporator. The oxygen source is a remote RF plasma generator which produces reactive oxygen atomic beams [5].

2.2.5 Block diagram of thin film deposition techniques

All the deposition techniques being used in the thin film technologies are categorized as two main type of deposition techniques, such as, physical vapor deposition (PVD), and chemical vapor deposition (CVD), which are shown in the block diagram (Fig. 2.1) as below:

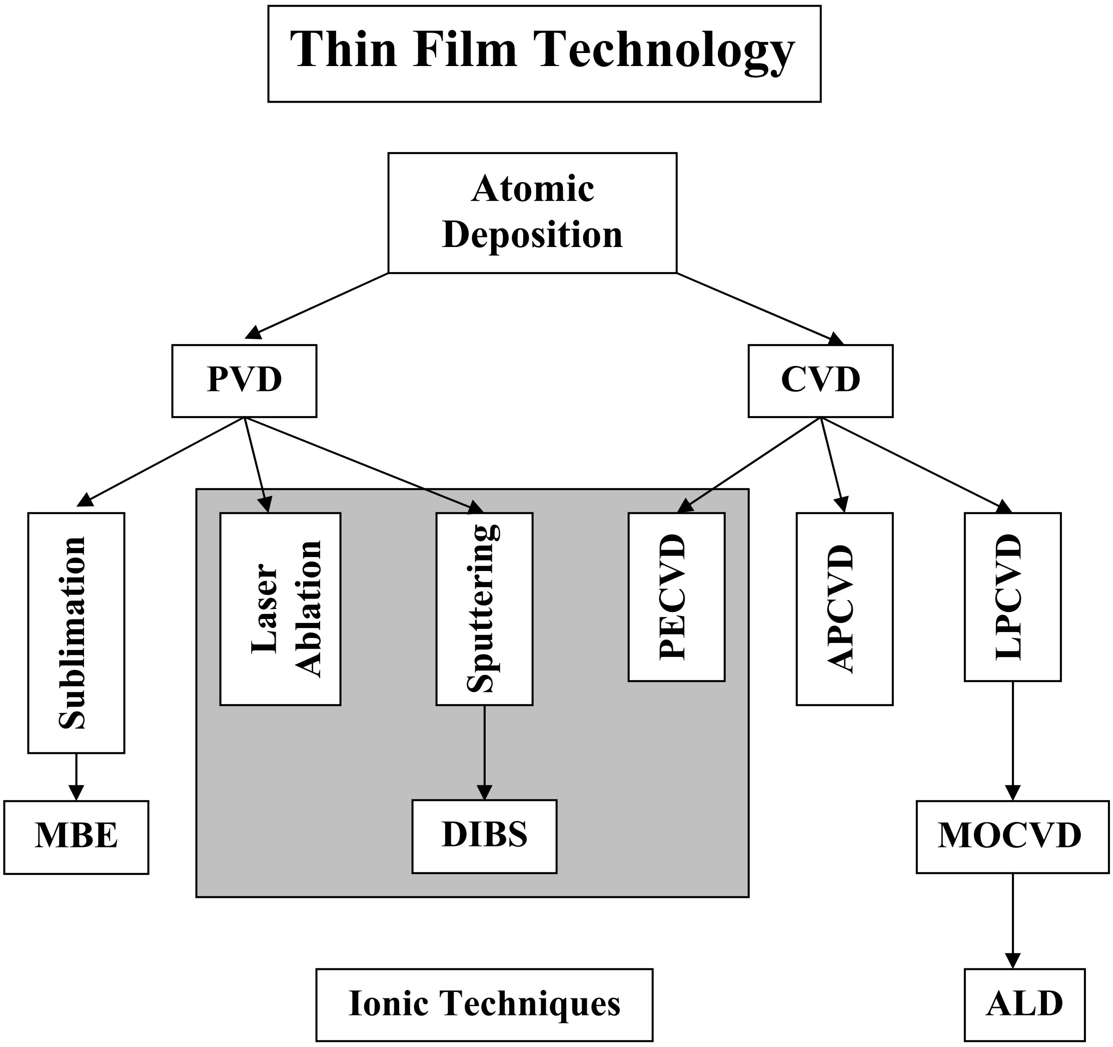
Thin Film Technology
Atomic Deposition
PVD
CVD
Sublimation
Laser Ablation
Sputtering
PECVD
APCVD
LPCVD
MBE
DIBS
MOCVD
Ionic Techniques
ALD

Fig. 2.1: *Block diagram of different deposition techniques are currently being used in the Semiconductors Technology on different substrates, such as Si, Ge, GaAs, etc. [After the talk of Prof. P. Patsalas, Department of Physics, University of Ioannina.]*

2.3 CMOS Processing

2.3.1 Introduction

The development of processing techniques for manufacturing ever-shrinking integrated circuits is the key to producing faster devices. The purpose of this section is to briefly discuss the deposition process considered for depositing a high-κ/metal gate stack and which have all been employed in the present work. The technique that used for depositing the gate dielectrics is MBE.

2.3.2 Germanium (Ge) Substrates Cleaning and Growth

One of the main components is the RF plasma source used for the generation of atomic oxygen beams with thermal energies, which are reactive enough to oxidize the impinging metals on the substrate at relatively low O_2 partial pressure in the 10^{-6} Torr range. Adequate preparation of Ge substrates prior to deposition is very important in order to obtain REOs (e.g. CeO_2, Dy_2O_3, La_2O_3, Dy_2O_3/HfO_2, and La_2O_3/HfO_2) films and interfaces with good electrical quality. As an ultrahigh vacuum (UHV) technique, molecular beam epitaxy (MBE) offers *in-situ* desorption of the native oxide, which cannot be achieved very easily by other more standard methodologies such as CVD. The substrate is heated to 360°C in vacuum until a (2×1) reconstruction spots appear on the screen is obtained by high-energy electron diffraction (RHEED), which is indicative of a clean Ge (100) surface (see Fig. 2.2). The source can produce also nitrogen and hydrogen atomic beams which can be used for surface treatment prior to growth in order to improve the electrical properties of the interfaces. Because MBE is a UHV technique it is possible to use RHEED for the *in-situ* realtime monitoring of native oxide desorption, surface treatment and growth. The main characteristics of this technique,(since no precursors are needed) is a flexible research tool for fast screening of a large number of complex metal oxides.

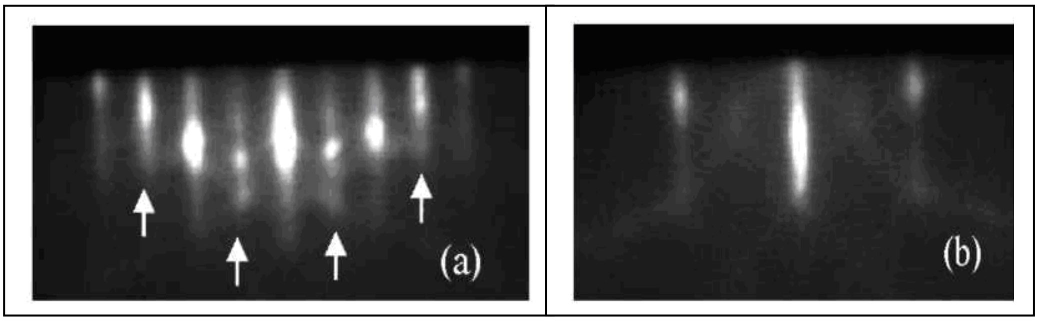

Fig. 2.2. *RHEED pattern of a clean Ge (100) surface. (a) along the (110) azimuth, (b) along the (100) azimuth, rotated by 45°. The weaker spots shown by arrows in (a) & (b) are diffraction spots due to (2x1) reconstruction of the surface. After ref. [6]*

2.3.3 Outlines of Sample formation and annealing

A general outlines for the MOS capacitors formation and anneal processing is shown in Fig. 2.3. The processing follows that of the single gate dielectrics (REOs) as well as gate stacks (HfO_2 together with REOs as interfacial buffer layer) in standard MOSCAPs production. This section describes those processes involved in creating the MOSCAPs and the subsequent annealing of the devices.

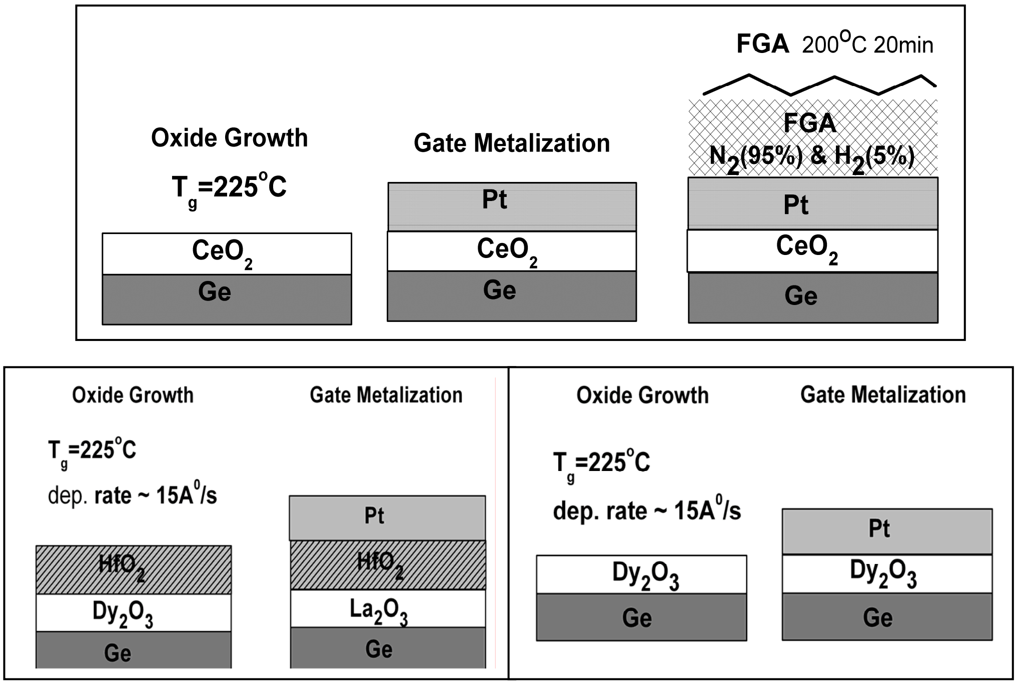
FGA 200°C 20min
Oxide Growth
T_g=225°C
Gate Metalization
FGA
N2(95%) & H2(5%)
Pt
CeO2
Ge
Oxide Growth
Gate Metalization
T_g=225°C
dep. rate ~ 15A°/s
Pt
HfO2
Dy2O3
La2O3
Ge
Oxide Growth
Gate Metalization
T_g=225°C
dep. rate ~ 15A°/s
Pt
Dy2O3
Ge

Fig. 2.3: *General outlines for MOS capacitors formation and anneal processing.*

2.3.4 Growth of gate dielectrics:

In the present study, single gate dielectrics rare earth oxide, REOs (e.g. Cerium Oxide (CeO_2), Dysprosium oxide Dy_2O_3, lanthanum oxide (La_2O_3) as well as REOs gate stacks, i.e. Dy_2O_3/HfO2 and La_2O_3/HfO2-based gate dielectrics are deposited using reactive evaporation in an ultrahigh vacuum (UHV) molecular beam epitaxy (MBE) system. The samples were prepared at the MBE Laboratory, Institute of Materials Science, NCSR, DEMOKRITOS, Athens Greece. Schematic and photograph of MBE system are shown in Fig. 2.4. (a) and (b) respectively.

The background pressure of the system is $< 1 \times 10^{-10}$ Torr and is maintained by using a turbomolecular pump, a cryogenic pump, and a titanium sublimation pump. Evaporation techniques available in the growth chamber, a single germanium e-beam evaporation source available for effusion cell sources. A rotating substrate manipulator/holder, capable of substrate heating to 1000 °C is situated at the center of the system. A brief description of the procedure as employed by this investigation is as follows: REO is evaporated using a high-temperature effusion cell at a temperature of 2000°C. During growth, the deposition pressure is maintained at 2 - 4×10^{-6} Torr by controlled high-purity oxygen flow using a mass flow controller.

Native oxides (CeO_2, Dy_2O_3, HfO_2/Dy_2O_3) were desorbed *in situ* under UHV conditions by heating the substrate to 360°C for 15 min until a (2×1) reconstruction appeared in the RHEED pattern, indicating a clean(100) surface. Subsequently, the substrate was cooled down to 225 °C where the oxide stacks were deposited. The substrate manipulator is typically maintained at 225 °C (although some experiments required variable deposition temperatures). A growth rate of ~ 0.15 Å/s was maintained at these conditions and monitored by quartz crystal rate monitoring. Extensive investigation of REOs grown by MBE on Ge substrates can be found elsewhere [6].

2.3.5 Metallization (Pt gate electrode)

The top gate electrode was prepared by e-beam evaporation of 30-nm-thick Pt using a shadow mask to define circular dots (200-1000) μm in diameter.

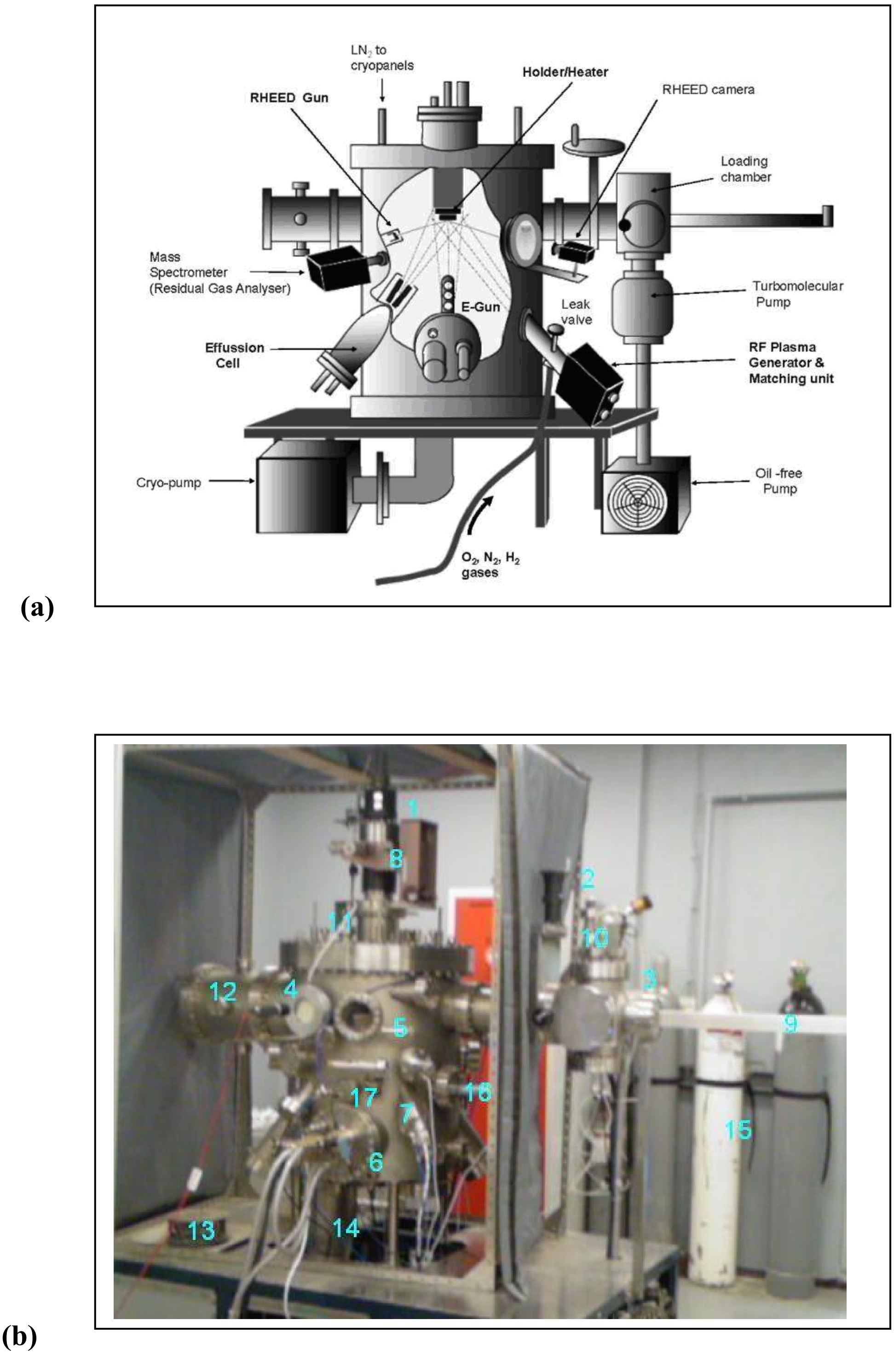
LN$_2$ to cryopanels
Holder/Heater
RHEED Gun
RHEED camera
Loading chamber
Mass Spectrometer (Residual Gas Analyser)
Turbomolecular Pump
E-Gun
Leak valve
Effusion Cell
RF Plasma Generator & Matching unit
Cryo-pump
Oil -free Pump
O$_2$, N$_2$, H$_2$ gases
(a)
1
8
2
11
10
12
4
3
5
9
17
16
7
15
6
13
14
(b)

Fig. 2.4: *(a) Schematic, (b) Photograph of molecular beam epitaxy (MBE) ultrahigh vacuum (UHV) system and components used for the growth of REOs base MOS devices at DEMOKRITOS in Athens, Greece. Base pressure ~5 x* 10^{-10} *Torr.*

2.3.6 Forming Gas Annealing (FGA):

A self developed FG system (detailed experimental setup is shown in the Fig. 2.5) at NSCR, DEMOKRITOS in Athens was used to anneal the samples at temperatures of 200-1200 °C for dwell times of 1 to 60 seconds.

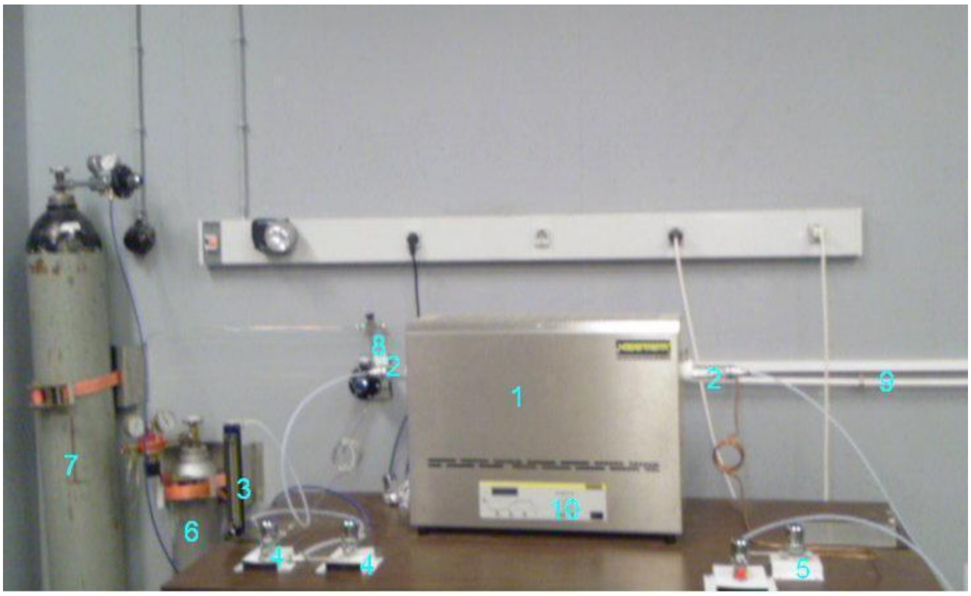

Fig. 2.5: Experimental setup of forming gas annealing (FGA) system at MBE Lab., NSCR, and Demokritos in Athens.

The temperature was monitored using a thermocouple attached to a germanium substrate that was capable of withstanding high temperatures. A ramp rate of 95 °C/s was possible from room temperature to 400 °C, followed by a 10 second dwell before ramping to 1200 °C. The anneal chamber was able to be sealed to allow for a flow of gas during the annealing process. Flowing gases available included a FG (Forming Gas with 95% nitrogen and 5% hydrogen), oxygen, nitrogen, and hydrogen. Initially, the extra attention is cleaning the pipe with gas nitrogen and afterwards the gas that needs is imported. A stable cool rate was not possible in the system, but the cool down was typically < 30 sec to achieve temperatures < 250 °C. The samples were removed once the temperature decreased below 200 °C. For some samples, a forming gas anneal was used in an attempt to passivate defects in the oxide and at the oxide/semiconductor interface. The forming gas anneal (5% H2, 95%N2) was typically 200°C for 20 min and was performed in a horizontal tube furnace with closed ends, so as to allow for gas flow during the annealing process. The samples were moved into the hot zone of the tube furnace after a sufficient time to allow the environment of the anneal chamber to be flushed with the forming gas (~5 min). After an anneal time of 30 min, the samples were removed to a cool end of the furnace and allowed to cool (< 100 °C) before purging the system with N_2 and removal from the furnace.

2.3.7 Back Ohmic Contact

In this work, indium-gallium (In-Ga) was used for a metal back contact in that it offers a lower electrical resistivity (compared to other the metal). Before attaching the samples on gold-plated chuck by In-Ga liquid alloy, the back side of the samples was scratched well with a diamond pen for having better surface contact, to reduce any parasitic series resistance. Finally all samples ware glued with silver paste on the top of gold chuck.

2.4 Experimental Techniques and Characterizations

2.4.1 Analytical characterizations

2.4.2 X-ray Diffraction (XRD)

XRD can be used to detect the transformation of the high-κ gate dielectric film from amorphous to polycrystalline state [7-11]. As the annealing temperature increases, the film may transform into a well organized polycrystalline phase, which shows defined XRD peaks [12]. By comparing the XRD patterns to the reference, the crystal structures can be identified.

For the XRD instrumentation, the most common X-ray source is a monochromatic CuKα X-ray (λ = 1.5418 Å). In addition, with the XRD information such as peak location and width (FWHM), the averaged crystallite (grain) size can also be estimated. The XRD data was performed at the Institute of Material Science, NCSR, DEMOKRITOS, Athens, Greece.

2.4.3 X-ray Reflectivity (XRR)

X-ray reflectivity (XRR) is a surface-sensitive analytical technique used in chemistry, physics, and materials science to characterize surfaces, thin films and multilayer [13-15]. It is related to the complementary techniques of neutron reflectometry and ellipsometry. The basic idea behind the technique is to reflect a beam of X-rays from a flat surface and to then measure the intensity of x-rays reflected in the specular direction (reflected angle equal to incident angle). If the interface is not perfectly sharp and smooth then the reflected intensity will deviate from that predicted by the law of Fresnel reflectivity. The deviations can then be analyzed to obtain the density profile of the interface normal to the surface. The thicknesses of each film (e.g. CeO_2, La_2O_3/HfO_2) were evaluated from high resolution X-ray reflectivity (XRR) measurements at the Institute of Material Science, NCSR, DEMOKRITOS, Athens, Greece, while XRR for Dy_2O_3, Dy_2O_3/HfO_2 was done at FRM-II of the Technical University of München, Germany.

2.4.4 Transmission Electron Microscopy (TEM):

A transmission electron microscope in principle is somewhat similar to an optical microscope [16]. It contains a series of lenses, which magnify the sample with a very high resolution of around 0.15 nm. This high resolution comes from the extremely small wave length of the electron, i.e., ~0.004 nm. The magnification of TEM can be several hundred thousand times. However, the limited depth of resolution is its main drawback, which requires an extremely small sample thickness (10-100 nm) for electrons to transmit. This increases the difficulty of sample preparation.

Three TEM imaging modes are available: bright-field, dark-field, and high resolution (HR). The TEM image contrast does not depend on the absorption, but on the scattering and diffraction of electrons. Images formed only by the transmitted electrons are bright-field images, and images formed by the diffracted beam are dark-field images. The image contrast is affected by mass contrast, thickness contrast, diffraction contrast, and phase contrast [16]. A high-resolution TEM (HRTEM) offers structural information on the atomic level, i.e., lattice imaging, which can be used for interface analysis. It contains a number of different diffracted beams, which combine together to form an interface image. In this work TEM was performed at the Institute of Material Science, NCSR, DEMOKRITOS, Athens, Greece, and was used a Philips CM20 with high resolution and Energy Dispersive X-ray Spectrometry capabilities.

2.5 MOS Electrical Characterization and Experimental Setup:

2.5.1 Introduction

For the electrical characteristics and reliability measurements of rare earth oxides (REOs) as dielectrics and/or an interfacial layer together with high-κ materials, i.e. gate stacks, which described in this thesis, we used a Keithley 617 electro-programmable meter, an HP 4284A multi-frequency LCR meter and our self-developed temperature controlled systems (see Fig. 2.6). The samples were heated with a hot chuck using a temperature-controller) and also held at a constant temperature, and/or at room temperature for a period of time during measurements. Fig. 2.6 shows a schematic diagram of the whole measurement process, while a detailed experimental setup in the Laboratory is illustrated in Fig. 2.7.

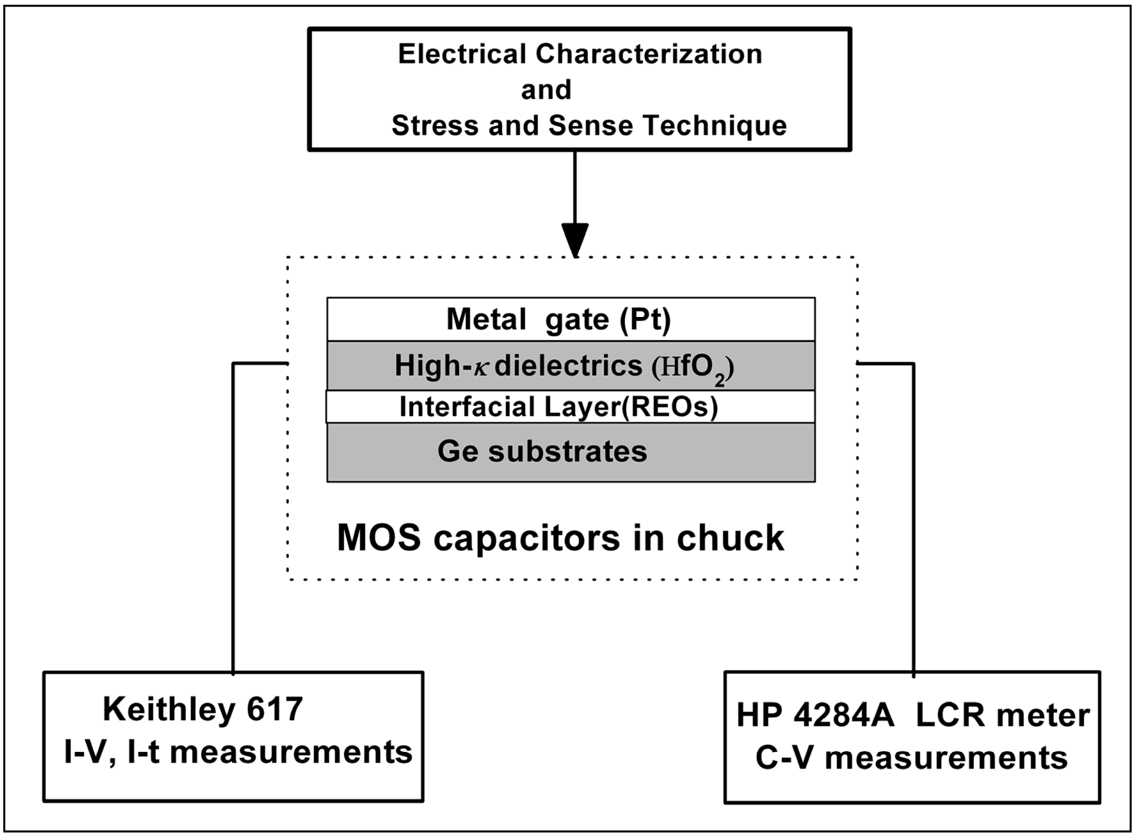
Electrical Characterization
and
Stress and Sense Technique
Metal gate (Pt)
High-κ dielectrics (HfO_2)
Interfacial Layer(REOs)
Ge substrates
MOS capacitors in chuck
Keithley 617
I-V, I-t measurements
HP 4284A LCR meter
C-V measurements

Fig.: 2.6 *Schematic diagram of the whole measurement system.*

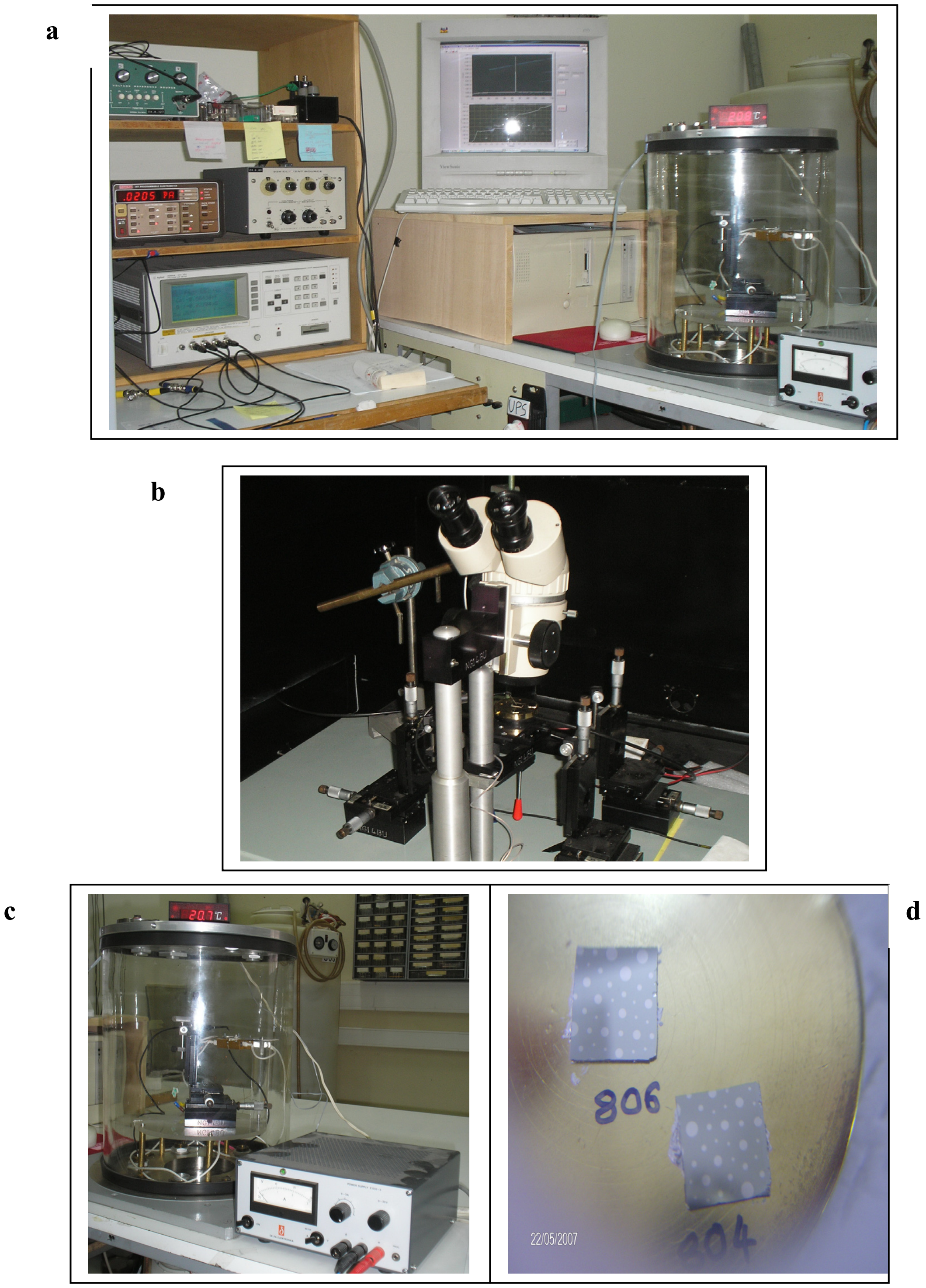
a
b
c
d
806
804
22/05/2007

Fig. 2.7: *(a) Measurements system, (b) probe station, (c) Temperature-controller system (d) Samples (Pt/CeO_2/p-Ge) on gold-plated chuck.*

2.5.2 Capacitance-Voltage (C-V) measurements

Electrical testing of capacitance and conductance with respect to the voltage applied to the gate electrode (*C-V* and *G-V*, respectively) was performed using an HP 4284A impedance analyzer. A first probe was placed in contact with the top layer of the capacitor and a second the back contact was made by In-Ga alloy on germanium substrates. Small area of capacitors (diameter 200~300 μm) were employed for reliability tests, and *C-V* curves recorded from 20 Hz to 1MHz (Fig.2.8) using step voltage of 0.05 V in the measurement.

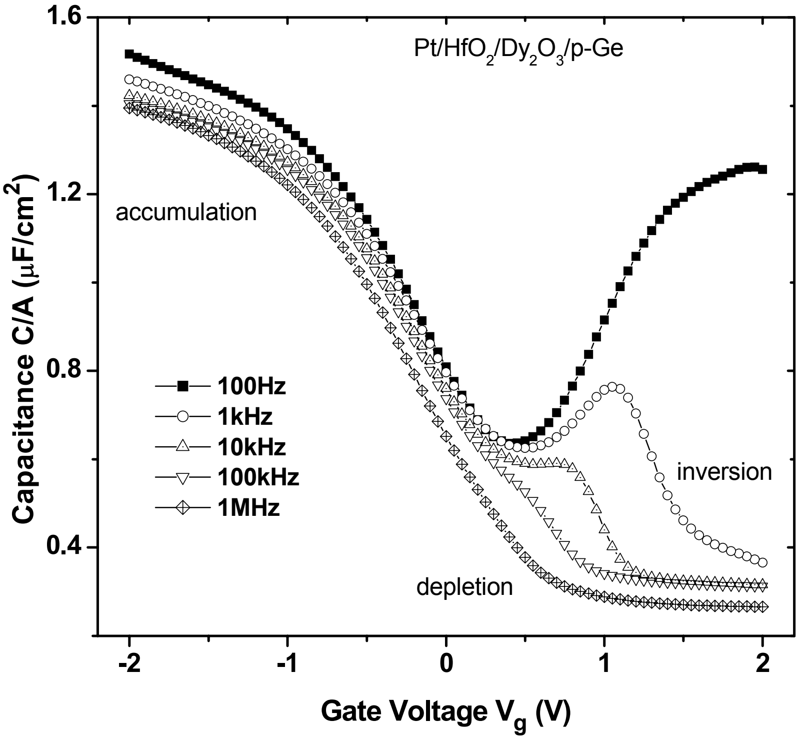

Fig. 2.8: *Capacitance–voltage (C-V) characteristics curve of Pt/HfO2/Dy2O3/p-Ge at different frequencies (20Hz-1MHz) at room 295K.*

The equivalent oxide thickness (*EOT*) was obtained from the high frequency (100 kHz) *C-V* curves using a simulator, MISFIT program [17] which solves Poisson and Schrödinger equations self-consistently, taking into account quantum confinement effects. The input of MISFIT program is high frequency *C-V* and *G-V* data and we get the output of *EOT.* Oxide trapped charges, $Q_{ox} = C_{ox}\Delta V_{FB}$ [18] and ΔV_{FB} due to successive CVS were obtained by analyzing the *C-V* curves at flatband capacitance (C_{FB}). Before stress, at fresh devices, the *C-V* curves were taken from inversion to accumulation and backward in order to avoid the deep-depletion effect [16].

For definiteness we assume that the change in the flatband voltage shift is due to interface trapped charge located at the gate stack/substrate interface and charge buildup in the bulk of the oxides. The trapped charge, ΔN_{ox} can be calculated using:

$$\Delta N_{ox} = -\frac{C_{ox}}{qA}\Delta V_{FB}\,, \tag{2.1}$$

where ΔV_{FB}, the flatband voltage shift, C_{ox} in oxide capacitance, q the elementary charge, and A the capacitor area. ΔN_{ox} was then plotted versus time or injected charge, Q_{inj}. (*Fig. 2.9*).

Trapped charge calculated from the change in flat band voltage is an approximation of the charge located in the insulator structure. However, since charge can be generated in places other than at the germanium-insulator interface, stress and *C-V* measurements only give a rough estimate of how much is trapped due to injected charges.

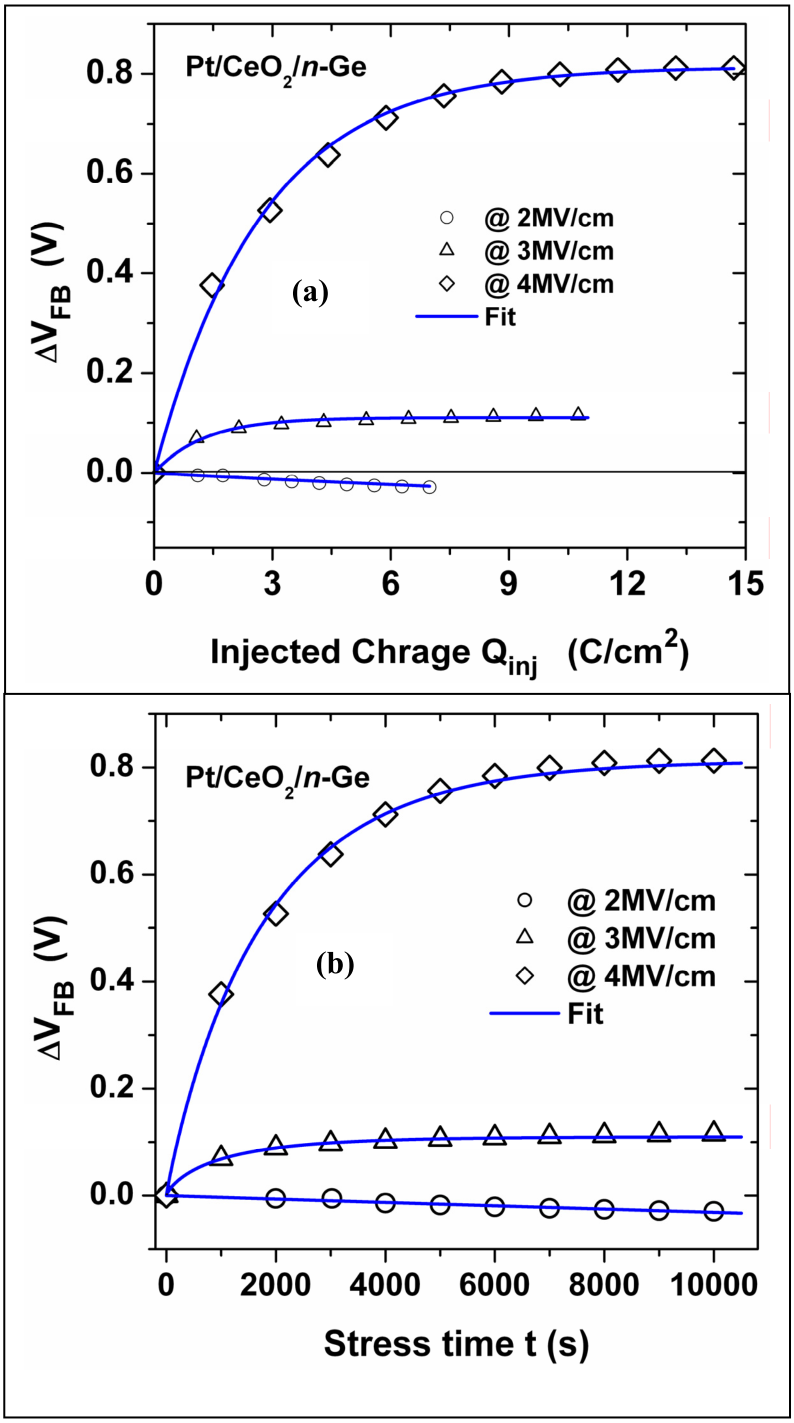

***Fig. 2.9 : F**latband voltage shifts (ΔV_{FB}) as (a) a function of stressing time (t) and (b) total injected charges (Q_{inj}) respectively under different CVS condition on Pt/CeO$_2$/n-Ge device. Experimental fit is according to Eq. (1.32) & (1.33)*

This measurement technique has the advantage of being simple and direct. It measures the effect of trapped charges from the *C-V* curve shift along the voltage axis as a function of injected charges. The stress was done in accumulation mode, so the injected charge was from substrate. However, it is essential to avoid relaxation of trapped charges during the stress cycle. If trapped charges de-trap too fast, some of the trapped charges may be lost during switching between the stress and *C-V* measurements. Minimizing the switching time is the key to success in this measurement. Another drawback with *C-V* is that it measures the combination of traps initially in the film in addition to those created later by the stress.

In most cases high-κ dielectric films have a high density of interface states (D_{it}) that results in an inflection in the *C-V* curve. As a matter of fact at low frequency (<10 kHz) *C-V* curves show a bump (see Fig. 2.8) which is due to D_{it} that respond to the ac-conductance [19].

2.5.3 Density of Interface States (D_{it})

The density of interface states, D_{it}, can be determined from an MOS capacitor by the use of the ac-conductance method [19]. The method involves measuring the complex admittance of an MOS device as a function of frequency at a number of different voltages, which has been discussed earlier in section § 1.7.

2.5.4 Current-Voltage (*I-V*) measurement

In a similar way to the *C-V* measurement, the leakage current was measured with respect to applied gate voltage (*I-V*) using a Keithley 617 programmable electrometer. The step was taken to ensure that the leakage was known with respect to the accumulation state of the MOS devices. *I-V* measurements were preformed on fresh devices and after constant voltage stress, aim is, to calculate stress-induced leakage current (SILC), which has been described briefly in the previous chapter.

2.5.5 Current-time (*I-t*) transient measurement

During the CVS on MOS capacitors, in-situ, leakage current-time (*I-t*) transient curves were recorded. From the *I-t* curves the total injected charges (Q_{inj}) was calculated which has been discussed before in this chapter. Also from this transient we monitor the types of charges which are filled up in the pre-existing traps in the bulk of the oxides, hence, can calculate the capture cross-section (σ). *I-t* fast transient also gives information of initial charge buildup, as well as, the creation of new defects at constant stress bias, nevertheless, the stress-induced leakage current (SILC) can be monitored.

2.5.6 “Stress and Sense” Characterization Technique

As pointed out earlier, the technique has been used extensively in literature to study the instabilities in conventional SiO_2 based gate dielectrics, and is known as the "stress and sense" method. In this case, an initial sense measurement is carried out prior to stressing the devices. The stress is then interrupted periodically and a sense measurement is performed. A schematic drawing of the bias sequence in "stress and sense" procedure is shown in Fig. 2.10 as below.

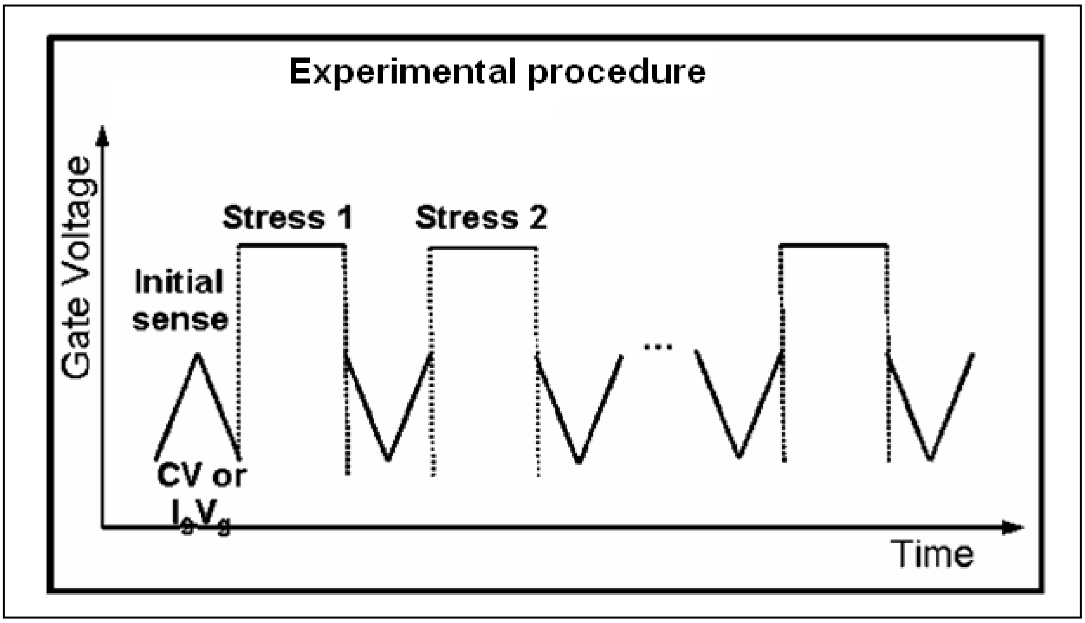

Fig. 2.10: *Waveform of the applied voltage versus time for a "stress and sense" technique. C-V and I-V sense sweeps are used in this thesis to monitor the flatband voltage shifts and total injected charges.*

The instability of the device is extracted by comparing the sense measurement after stress with the initial device characteristics. Predictions to operation conditions are usually made when combining the time dependence with the voltage dependence of the instability.

One of the known issues of the stress and sense procedure is the inherent time delay between stressing and sensing. In case, some recovery of the instability occurs at the time periods on the order of ~ 10 to 100 ms, this procedure will not capture its full extent. For high-*κ* gate stacks, where there is fast transient charging, a better way to quantify the instability is by monitoring gate leakage current degradation as and when the capacitor is stressed. The instability in the gate leakage current can come from either of the following two sources: a) loss or gain in inversion charge due to charge trapping effects, b) enhancement in the scattering mechanism due to generation of scattering centers like interface states.

As demonstrated earlier in this, a typical measurement for charge trapping is the *C-V* hysteresis and *I-V* characteristics along with *I-t* transient measurements to determine the flatband voltage shift, ΔV_{FB} and stress-induced leakage current, SILC. In particular, *C-V* hysteresis measurements can be used to monitor ΔV_{FB} shifts. However, this technique as a sole measurement of ΔV_{FB} has some drawbacks since the results strongly depend on the test conditions, that is the voltage sweep amplitude and ramp rate. To address this issue, a more quantifiable technique that uses a constant voltage gate dielectric stress (CVS) with interspersed limited-voltage-range *C-V* measurements around flatband can be used [20]. Although systematic, this technique results in the de- trapping of some of the charge between the stress and sense sequence. Flat band voltage as a function of stress time or injected charge provides information on how much charge is trapped in the gate stack structure. Despite this limitation, this technique is chosen as a unique tool for detecting the full impact of stable trapped charge in high-κ based gate stacks.

First, 100 kHz C-V data was collected on both p and n-MOS capacitors (dielectrics of CeO_2, Dy_2O_3 and gate stacks, Dy_2O_3/HfO_2). The application and system components enable a constant voltage stress with interspersed limited-voltage-range *C-V* measurements of a few tenths of a volt around V_{FB} to minimize any additional stress. This *C-V* sweep could also be bi-directional to see any hysteresis related to the measurement itself. The ΔV_{FB} is then referenced from the initial limited-voltage range *C-V* measurement taken before stressing (i.e. *C-V* on fresh devices). This technique was applied to various REOs-based MOS capacitors in an effort to evaluate the charge-trapping nature of the respective films.

When the device under the voltage stress condition, leakage current is measured in an effort to quantify the amount of charge injected into the gate, which is expressed as:

$$Q_{inj} = \int_0^t I_{leakage} dt \qquad (2.2)$$

Between voltage stresses, two types of measurements can be done in sequence: *C-V*, and *I-V*, however, *I-t* transient was also *in-situ* measurement [21]. From these measurements, important device parameters can be extracted and plotted as a function of time to show the degradation caused under constant voltage stresses (CVS). From successive *I-t* transients under CVS one can measure SILC.

2.6 Reliability Measurements

2.6.1 Introduction

In-order to do reliability measurements we used different stresses methods. The measurement methods [22] commonly used in dielectric yield and reliability assessment are the following:

1. Constant voltage stress (CVS): constant voltage stress is used to measure the time to breakdown (t_{BD}) at different stress fields.
2. Constant current stress (CCS): Constant current stress is employed for the measurement of the charge to breakdown (Q_{BD})
3. Ramped voltage stress (RVS): Ramped voltage stress is used to measure breakdown fields (E_{BD}) and current-voltage (*I-V)* characteristics.
4. Exponentially ramped current stress (ERCS): This stress method is employed to obtain a fast measure of charge to breakdown (Q_{BD}), the breakdown strength (I_{BD} and E_{BD}) and the current-voltage (*I-V*) characteristics.
5. Combined ramped/constant stress measurements:

   These measurements are used to record extrinsic breakdowns and intrinsic times to breakdown with short measurement times and high resolution.

2.6.2 Details of the stress methods

The following subsections will describe in detail some listed stress methods which were employed in this work. In addition to a detailed description of the implementation and the performance of the stressing techniques a brief view of the historical background is given. Advantages and disadvantages and common problems are highlighted. Typical applications of the stress methods are discussed in later sections.

In the present work, among the above mentioned techniques, the following two techniques were employed, such as, Constant voltage stress (CVS), and Ramp Voltage stress (RVS) for analyzing the reliability issues. The following subsections will describe in detail the two methods. In addition to a detailed description of the implementation and the performance of the stressing techniques a brief view of the historical background is given. Advantages and disadvantages and common problems are highlighted. Below we briefly report on these techniques.

2.6.3 Constant Voltage Stress (CVS):

The constant voltage stress (CVS) is frequently used for the measurement of the time to breakdown, T_{BD}, and the extrapolation of oxide lifetimes at normal operating conditions from highly accelerated reliability stresses. Note that when the lifetime of an oxide is mentioned in the text it refers to the operating conditions, and time to breakdown (t_{BD}), refers to accelerated reliability measurements. Constant voltage is applied to the gate until oxide reach breakdown (*BD*) (rapid, irreversible increase of the gate current).

In the literature extensive investigations are reported using CVS with fields ranging from 3 to 12 MV/cm [23-28] and different temperatures from 25-400°C [29-33]. When low/moderate stress fields are applied to high quality oxides at room temperature, measurement times range in the order of days to months. In this case, the long term dielectric reliability is investigated with CVS and extrinsic as well as intrinsic breakdowns are recorded [24, 34-35]. Such long measurements can be done on packaged samples or at wafer level with a lot of devices stressed in parallel [23].

For wafer-level tests, it is usual to increase the field and/or the temperature to keep measurement times low, $t_{BD}<10{,}000$ s. As a consequence, at highly accelerated stress fields, very often dielectric structures with defects will break down at time zero and it will not be possible to record the extrinsic distribution. Therefore, it is mainly the intrinsic breakdowns which are monitored with CVS measurements at highly accelerated fields [26].

2.6.4 CVS measurement method.

The principle of the CVS, which is also referred to as TDDB (time dependent dielectric breakdown) measurement is straightforward. A constant voltage is applied to the dielectric under test. The current through the dielectric is measured until breakdown occurs. When the recorded current is plotted vs stress time the current-time (*I-t*) characteristic can be studied. Figure 2.11 shows a typical *I-t* curve for a thick oxide (SiO_2) [36-37].

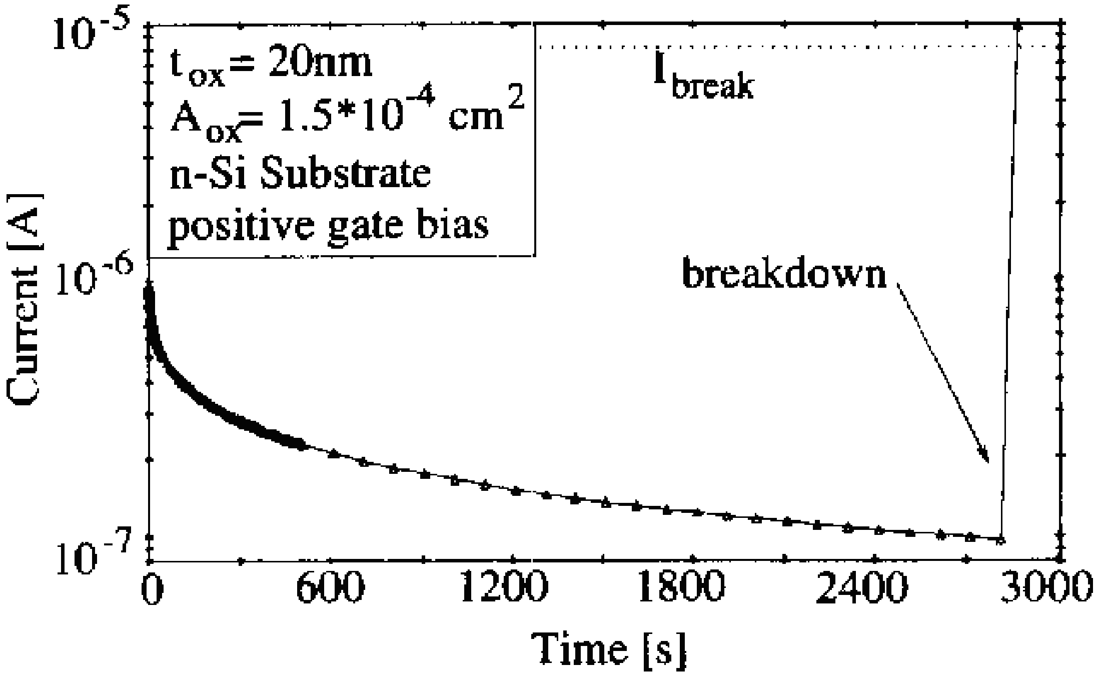

Fig. 2.11: Current-time characteristic for a 20 nm MOS gate oxide recorded during a CVS at 9.65 MV/cm. After ref. [30]

Dielectric breakdown is detected when the measured current rises by several orders of magnitude and/or reaches a pre-defined breakdown current ($I_{BD,}$ i.e. the current to breakdown of the MOS capacitor). It can be seen from the *I-t* curve in Fig. 2.11 that the measured current ultimately becomes bigger than I_{BD}.

Figure 2.11 shows that the leakage current I_g can be high for the initial part of the I_g-t curve due to initial rapid charge formation and it might be even necessary to introduce two I_g factors, one for the first few seconds and the other for the time until breakdown occurs which can be much smaller. The values for I_g are strongly dependent on the oxide charge trapping characteristics and the measurement parameters and must be assessed individually.

It is useful to record the current evolution during stress. The frequency of measured points determines the resolution of t_{BD}. Logarithmic sample periods are adequate for recording currents since the change in current with time is exponential. Figure 2.12 illustrates that an equal number of current readings per decade can be retained which keeps the amount of recorded data low [38], even for $I_{BD} > 100{,}000$ s. Figure 2.12 shows the same I_g-t data as plotted in Fig. 2.11. This way of presenting the I_g-t characteristics makes it possible to study the initial current evolution at the same time as the currents that flow shortly before breakdown.

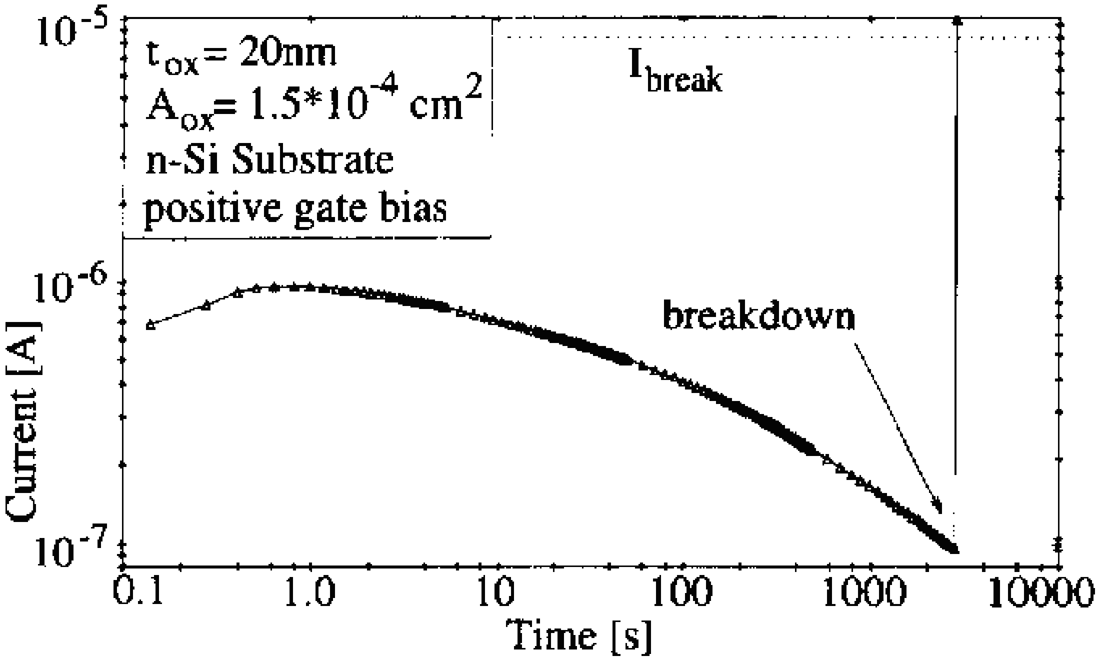

***Fig. 2.12**: Current time characteristics for the oxide of Fig 2.11 with current and time log scales. After ref. [29]*

In the present thesis this method is used to investigate the breakdown characteristics, charge trapping characteristics, to measure the stress-induced leakage current (SILC). For these measurements we have used various REOs based MOS devices grown on Germanium substrates which are mentioned before. With Keithley 617 electrometer we could take two samples reading per second.

2.6.5 SILC measurement under CVS

Stress-induced leakage current (SILC) is measured under CVS conditions. SILC is the increase in low-level leakage through thin dielectric layers, after the oxide has undergone a high electric-field stress. Stress-induced leakage current ($J_{SILC}=J_t-J_0$) is defined as the increase in oxide leakage current density after a high-field stress (J), as compared to the leakage prior to any stressing (J_0). Figure 2.13 is a typical example of how the low-level leakage current increases after the device has been stressed. The black solid line is the fresh current density (J_0) on Pt/CeO$_2$/Ge capacitor while the red solid line indicates the current density after CVS. The difference in current density is SILC as shown in the Fig 2.13.

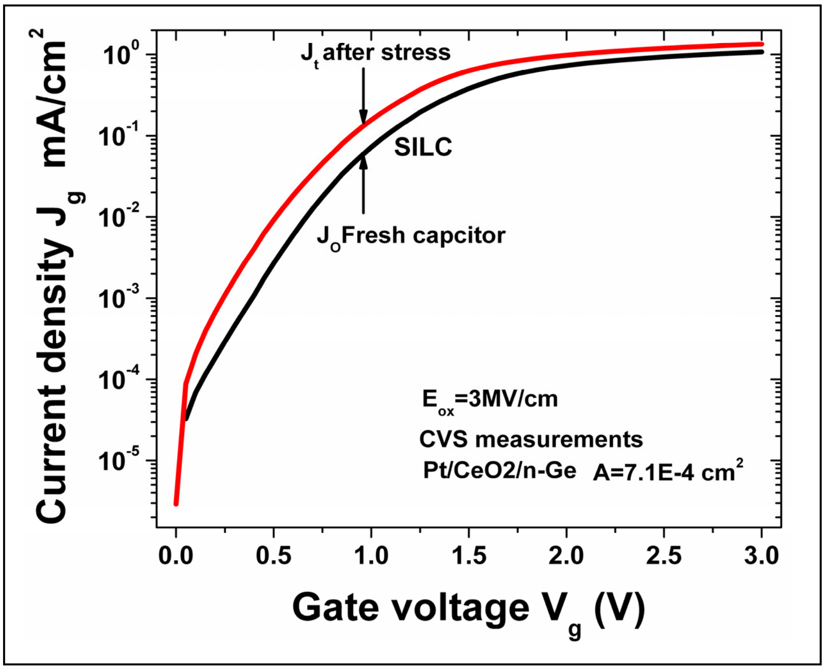

Fig. 2.13 : *Current density (J_g) as function of gate bias (V_g) curves on fresh device and after constant voltage stress (CVS), which illustrates stress-induced leakage current (SILC). The CVS was performed on Pt/CeO$_2$/n-Ge capacitor.*

2.6.6 Ramp Voltage Stress (RVS):

Ramp Voltage stress (RVS) is one of the so called wafer Level Reliability (WLR) tests. In RVS, voltage across an oxide is increased at a constant linear rate until failure occurs. The basis flow chart of Ram Voltage Stress (RVS) is given below occurs. The basis flow chart of Ram Voltage Stress (RVS) is given below occurs.

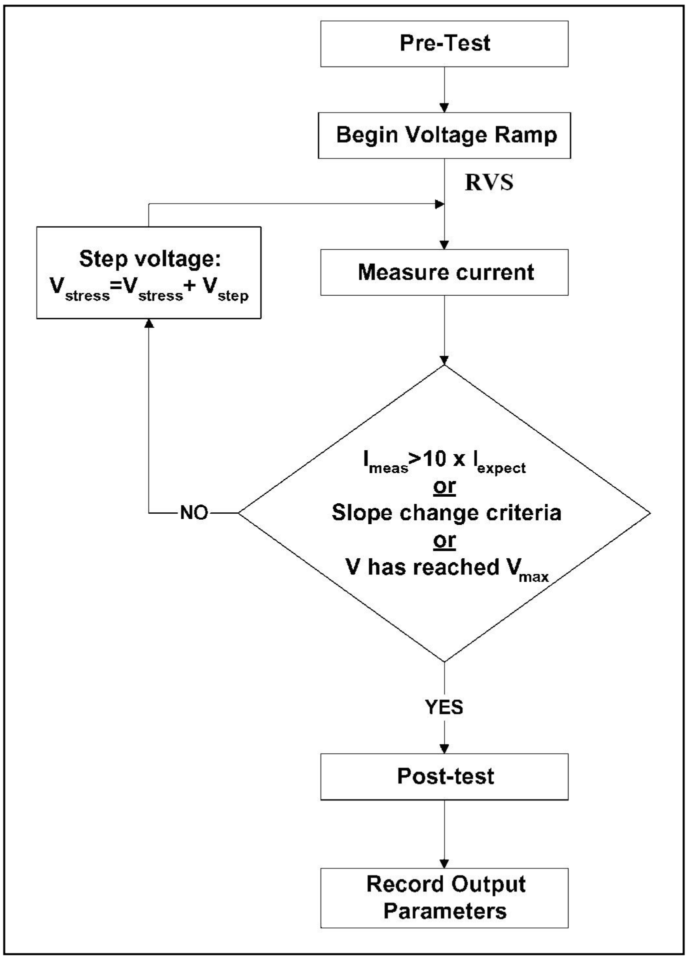
Pre-Test
Begin Voltage Ramp
RVS
Step voltage: $V_{stress} = V_{stress} + V_{step}$
Measure current
$I_{meas} > 10 \times I_{expect}$ or Slope change criteria or V has reached V_{max}
NO
YES
Post-test
Record Output Parameters

Fig. 2.14: *Basic block diagram of Ramp Voltage Stress (RVS) in the diagram.*

This is more sensitive at detecting breakdown (*BD*) at lower voltages; also it is more commonly applied to test structures which may have relatively large oxide areas equal to that of an entire semiconductor integrated circuit or larger. It records total charge (Q_{BD}), time to breakdown (t_{BD}) and as well as breakdown voltage (V_{BD}). These parameters are measured on a large number of test samples and usually plotted as cumulative breakdown distribution versus breakdown charge density or breakdown electrical field on probability chart. The manufacturing process should be maintained so that this distribution becomes closer to the ideal shape. RVS is more sensitive at detecting breakdown at lower voltages (i.e. logic, microprocessors) and which plays an important role to characterize of the reliability of the devices. We use a few RVS measurement for each sample to get the breakdown caracteristics because we did not have many samples to do Weibull plot as this RVS finally reach beakwond.

The accumulated charge passing through the oxide prior to breakdown is defined as:

$$Q_{BD} = \int_{t=0}^{t=t_{BD}} I(t)dt, \tag{2.3}$$

where t is time. The Q_{BD} is calculated as the integral from $t = 0$ to $t = t_{BD}$; where t_{BD} is the last measurement time at the step just prior to breakdown. If the area of the capacitor is A, then the accumulated charge density Q_{BD}, passing through the oxide at the detection of breakdown (Q_{BD}) can be written as:

$$q_{BD} = \frac{Q_{BD}}{A}, \tag{2.4}$$

From the following Fig. 2.15 these are illustrated briefly the RVS mechanism and monitoring of the charge to breakdown Q_{BD} characteristics which is an important parameter of reliability characteristics of MOS devices. Figure 2.16 shows the RVS experimental results on $Pt/HfO_2/Dy_2O_3$/p-Ge capacitor of area of 3.14×10^{-4}cm.

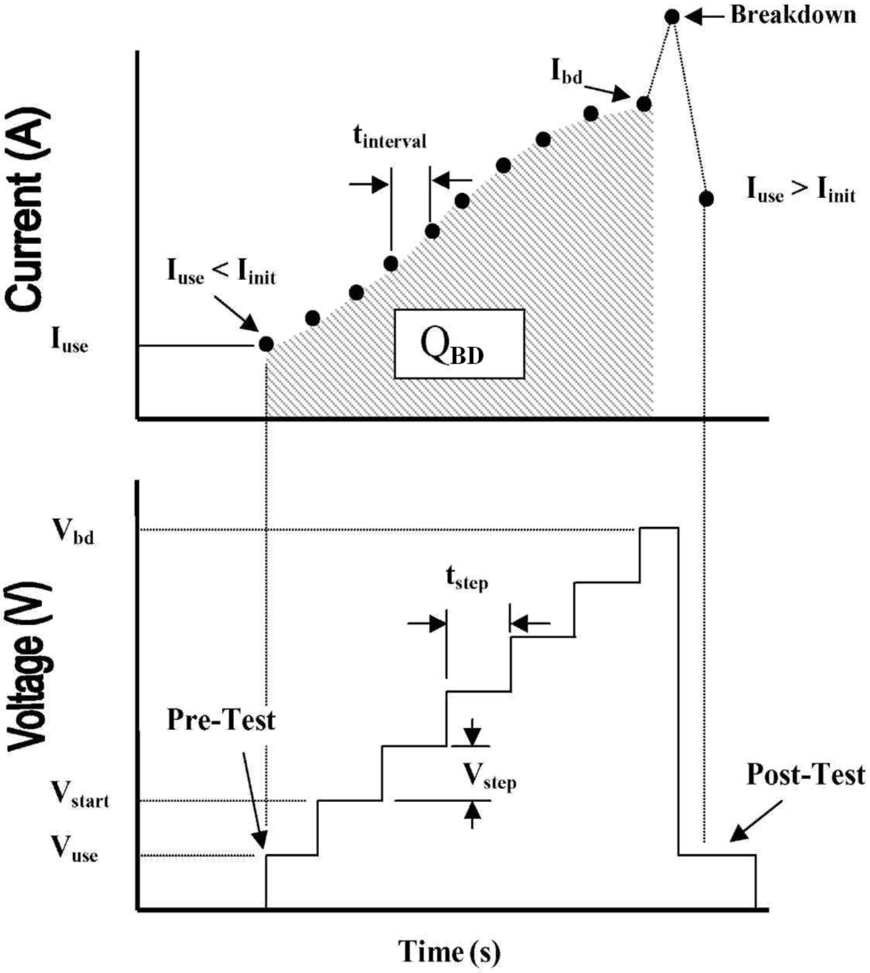
Breakdown
I_bd
t_interval
I_use > I_init
I_use < I_init
Current (A)
I_use
Q_BD
V_bd
t_step
Voltage (V)
Pre-Test
V_step
V_start
Post-Test
V_use
Time (s)

Fig. 2.15 *Typical illustration ramp voltage stress when applied to the MOS capacitor calculation of Charge to Breakdown (Q_{BD}) from the measurements.*

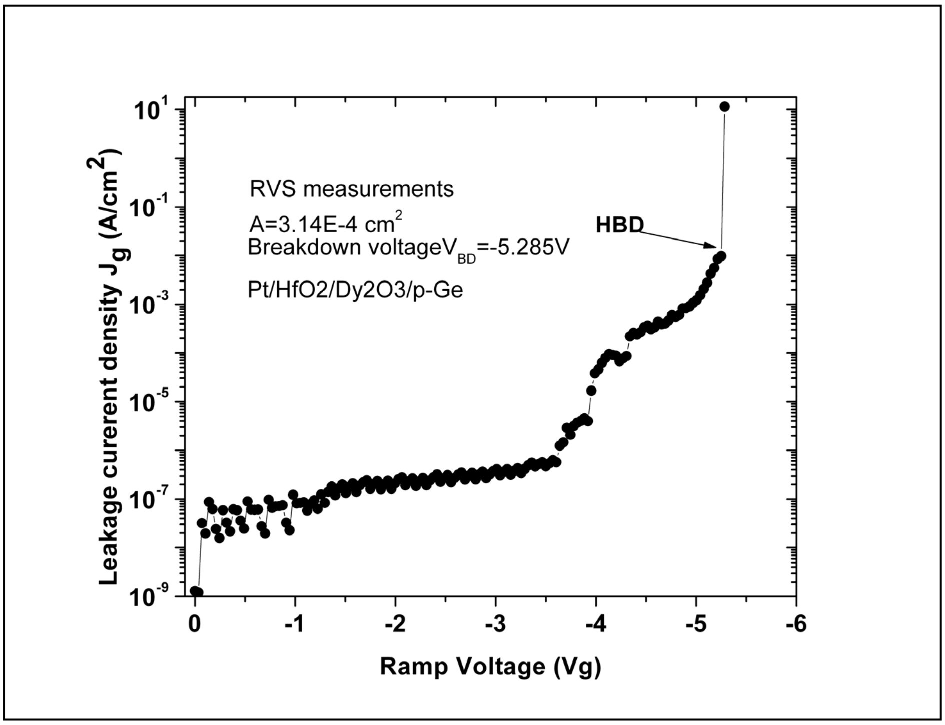

Fig. 2.16: *The application of ramp voltage stress (RVS) was preformed in this work on Pt/*HfO_2*/*Dy_2O_3*/p-Ge capacitor of area of* 3.14×10^{-4}*cm. Breakdown voltage* V_{BD} *=-5.8V*

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Chapter 3

“Anomalous Charge Trapping Dynamics, and correlation of charge buildup and SILC in Cerium Oxide grown on Germanium substrate”

3.1 Motivation

We have investigated charge trapping phenomena in thin films of cerium oxide on *n*-type germanium (Ge) substrate under constant voltage stress (CVS) condition. We try to find the correlation of the charge trapping characteristics and the stress induced leakage current (SILC) to the applied field in this chapter. The results we observe suggesting that one major problem for the potential use of rare earth oxides in future MOS technology is the existence of relaxation effects. The cross section value of the bulk oxide traps is of the order of 10^{-18} cm^2, thus indicating neutral defects. Direct comparison to reported results on high-κ/Si and SiO_2/Si structures shows that SILC properties are related to the quality of the dielectric layers; the semiconductor substrate is immaterial.

3.2. Experimental

Thin insulating films of CeO_2 were grown on n-type Ge (100) substrates using molecular beam deposition (MBD). There are different sizes of MOS capacitors in diameter 300nm to 1000nm are use in this study. For reliability measurement we used smallest diameter capacitor of area 7.1×10^{-4} cm^2. Different CVS were applied, for example ranging from 0.7V to 4.0V were for charge trapping, stress-induced leakage current (SILC), border traps characteristics, and to determination of capture cross-section of trap analysis. All the measurements were at room temperature. The MOS diodes have been characterised electrically by means of capacitance-voltage (*C-V*), conductance- voltage (*G-V*) and current-voltage (*I-V*) measurements which were performed before and after annealing. Consequently, the devices have been subjected to electrical stress under constant voltage stress conditions (CVS), whereas the *C-V* and *I-V* curves were measured after each stress cycle using an Agilent 4284A LCR meter and a Keithley 617 electrometer. Charge trapping and SILC were studied by measuring flatband voltage shift (V_{FB}) of high frequency (100 kHz) capacitance–voltage (*C–V*) curves as a function of charging time (or injected charge) and current-time (*I-t*) transient respectively by using a pulsing (also known as ''stress and sense'') technique shown in Figs. (1) and (2). Border traps characteristic was analyzed by using fresh *C-V* and *C-V* after stress.

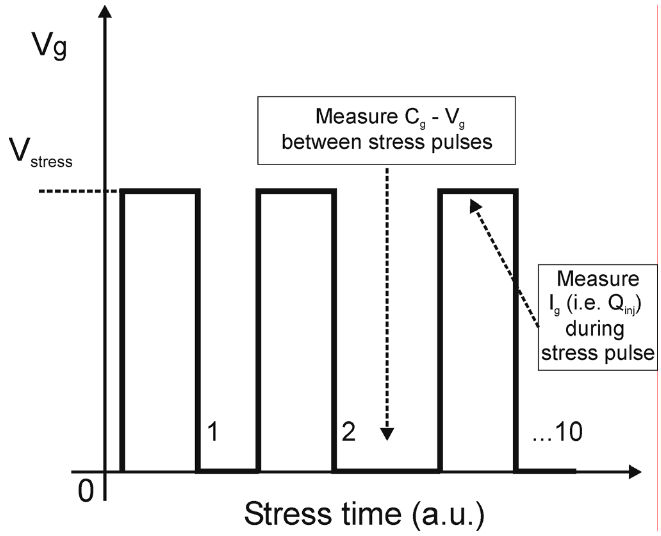

Vg
V_{stress}
Measure C_g - V_g between stress pulses
Measure I_g (i.e. Q_{inj}) during stress pulse
1
2
...10
0
Stress time (a.u.)

Fig.1. *Illustration of the 'pulsing technique' used for charge trapping measurements.*

The applied field (E_{ox}) across dielectric (CeO_2) was calculated by $E_{ox} = V_{ox}/t_{ox}$, where $V_{ox} = V_g - V_{FB}$ is the voltage applied to the gate dielectric stack, V_g is the gate bias voltage; V_{FB} is the flatband voltage.

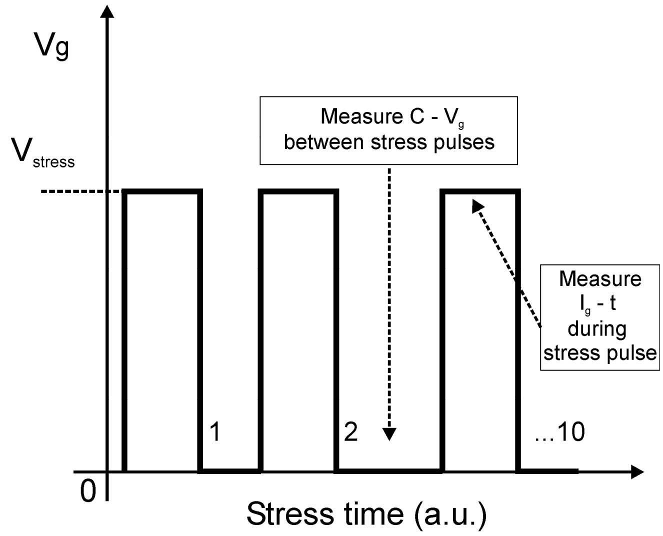

Vg
V_stress
Measure C - V_g between stress pulses
Measure I_g - t during stress pulse
1
2
...10
0
Stress time (a.u.)

***Fig. 2:** Illustration of the ''stress and sense'' technique used for charge build-up and SILC measurements.*

A. Anomalous Charge Trapping Dynamics in CeO_2

3.3. Results and Discussion

3.3.1. *C-V* and *I-V* measurements

Initially the MOS devices were characterized by means of the analysis of conventional *C-V*, *G-V* and *I-V* curves. Figure 3 shows the *C-V* characteristics of the films before and after annealing. A number of films have been grown at the same growth conditions with the physical thickness of the oxide d_{ox} (ranging between 7 to 14 nm) as the only changing parameter. Following a typical analysis for the evaluation of the equivalent oxide thickness (*EOT*) for each film and a plot of EOT vs d_{ox} we obtained the dielectric constant of the ceria films (κ_{ox} = 23) [1]. While the calculated κ value is very good, the existence of a defective interfacial layer with physical thickness between 1~2 nm and a dielectric constant κ_{il}= 11 was also obtained from the same plot [2]. This interfacial layer was also confirmed from high resolution TEM measurements [1-3]. This rather thick interfacial layer is probably the reason for the high density of oxide defects of the corresponding MOS devices and proper annealing treatments is currently under investigation in order to benefit from the

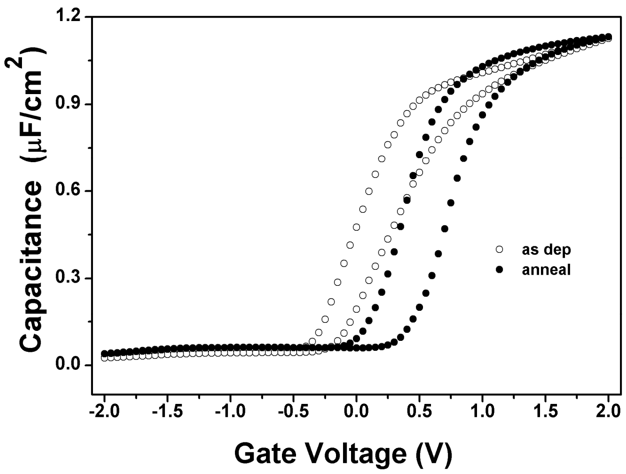


Fig. 3. *C-V of as deposited and annealed at 200°C samples measured at f=1MHz.*

high-κ value of the ceria films after proper passivation of the Ge/Ceria interface. The existence of this layer will be also taken into account in the next paragraphs dealing with the trapping phenomena. It should be emphasized here that in the present work we report on the electrical characteristics and the related trapping phenomena of one set of samples with physical oxide thickness around 10nm as mentioned before.

A comparison of the 1MHz *C-V* curves in Fig. 3 shows a negative charge trapping after annealing in forming gas. When the flat band voltage shift is used to quantify the amount of trapped charge, it is the bulk oxide charge that is -usually- probed. On the contrary, when the width of the hysteresis loop is under examination, it is the amount of “border traps” [4] being investigated. The latter case will not be examined in this work. However, the amount of the bulk oxide trapped charge before and after annealing could be obtained from the high frequency (*hf*) *C-V* curves. The calculated value of Q_{ot} (= $\Delta V_{FB} C_{ox}$= 3.06×10^{-7} C cm^{-2}) is rather high and reflects the poor quality of the semiconductor/oxide interface.

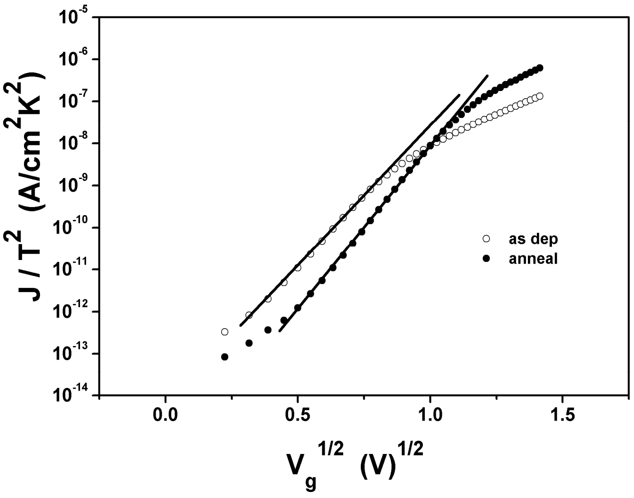


***Fig 4**. Current-Voltage characteristics of as-deposited and annealed Pt/CeO_2/n-Ge devices measured at T=297K. The solid lines are simply guide to the eye for Schottky type current transport at low voltages.*

Figure 4 illustrates the current density as a function of applied bias for both as deposited and annealed samples. The current transport through the ceria film is due to the Schottky mechanism for low and medium fields (corresponding V_g in the range 0–1V) while at higher fields it is the Poole-Frenkel (P-F) conduction [5] that best describes the experimental data. It is also obvious that the current density at V_g=1V is quite high (around 1mA/cm^2). This is consistent with previously published data on ceria films [6] which show that the high leakage currents are mainly attributed to the relatively small energy gap of the oxide (E_g = 3.3V). After annealing the onset of P-F conduction moves to slightly higher gate voltages, which is consistent with a reduction of the amount of bulk oxide and interface defects. However, as the present work focuses on the trapping dynamics of the corresponding structures, we did not study the current conduction mechanisms with temperature in order to obtain more precise quantitative results.

3.3.2. Constant Voltage Stress (CVS) measurements

Only the annealed samples were stressed under CVS condition [7-9]. In general, the flatband voltage shift due to trapped charge in the oxide is given by [10]

$$\Delta V_{FB} = -[\frac{q}{C_{ox}}]\int_0^d \frac{x\Delta\rho(x)}{d_{ox}}dx \qquad (3.1)$$

where C_{ox} is the oxide capacitance, d_{ox} is the oxide physical thickness, x is the distance from gate electrode to trapped charge sheet, and $\rho(x)$ the spatial charge density inside the oxide. The integral limits are taken from 0 to d_{ox} measured from the gate electrode. It is clear that a positive charge density results in a negative flatband voltage shift while the opposite is true for negative trapped charge.

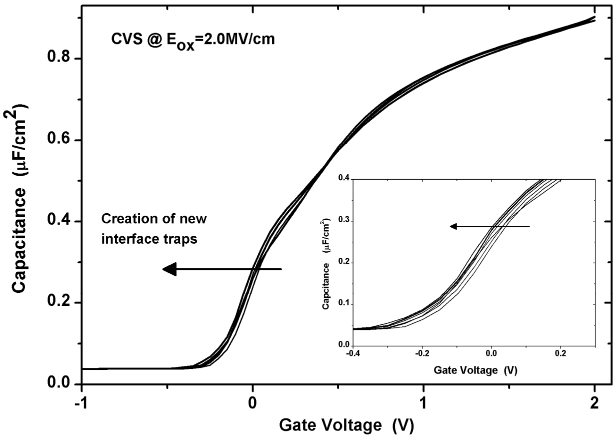


Fig. 5. *High frequency C-V curves (f=100KHz) of annealed films measured after CVS at a corresponding E_{ox} = 2 MV/cm. The arrow indicates direction of flatband voltage shifts, ΔV_{FB} over time during stress. The insert shows an enlarged view of the curves around V_{FB} for shake of clarity.*

Charge trapping was studied by measuring flatband voltage shift ΔV_{FB} of high frequency (100 kHz) capacitance-voltage (*C-V*) curves at various electric fields (ranging from 2.0MV/cm to 4.0MV/cm) for a constant stress time interval equal to 1000s. The applied voltages biased the devices at strong accumulation (i.e., injection of electrons from the germanium substrate), while all measurements were done at room temperature. Fresh diodes were used for each stress measurement (low field and high field). In Fig. 5 a negative flatband voltage shift ΔV_{FB} in the depletion region of the *C-V* curve is observed at the lower stress field used ($E_{ox} \approx$ 2MV/cm). This shift can be attributed to trapping at the interface states and is consistent with the corresponding "lowering" of the curves at strong accumulation. A conventional analysis of the "stretch-out" effect of the high frequency *C-V* curves due to higher D_{it} values can be found in any standard textbook [11].

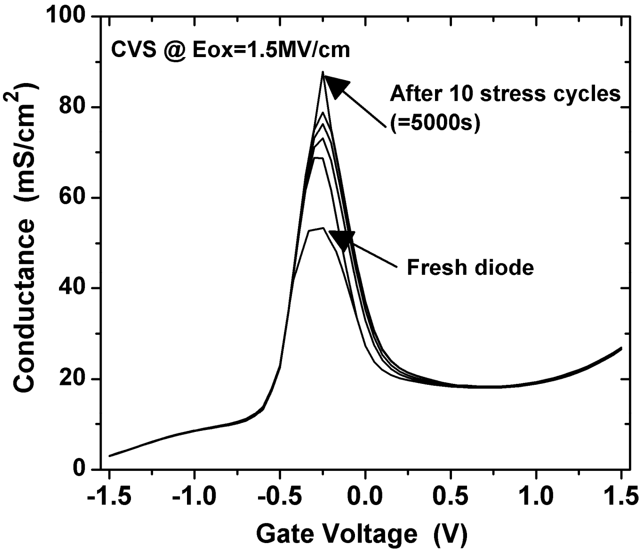


Fig. 6. *Conductance (G) vs gate voltage (V_g) curves (f=100KHz) measured after CVS at a corresponding E_{ox} =1.5MV/cm. Each curve was acquired after a 500s long stress cycle. Not all data are plotted for clarity.*

The study of the hf ac-Conductance vs V_g *(G-V)* measurements was then used as a tool to identify the location of the positive charge. Fig 6 shows the corresponding *G-V* plots for the devices stressed at a low ($E_{ox} \approx$ 2MV/cm) field, while Fig 7 shows the evolution of the maximum *G* value (G_{max}) after each stress cycle for all three oxide fields studied. It should be mentioned here that the procedure followed for this experiment consisted of two steps: (i) application of a stress voltage at accumulation for a time interval of 500s or 1000s and (ii) *C-V* measurement sweeping from inversion to accumulation. In this way, all the trapping effects due to the application of a positive V_g were cancelled whereas any new, stress-induced interface defects

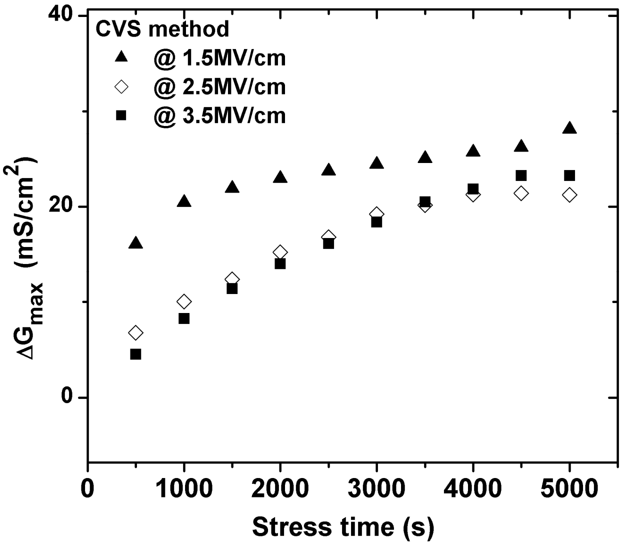


Fig. 7. *Change of the Conductance peak (ΔG_{max}) versus stress time (t) for different E_{ox} stress values.*

were detected by the change of the corresponding ac-*G* peaks. From Fig. 7 it is rather clear that the G_{max} peak, which is related to the presence of interface states, is almost one order of magnitude greater than in the case of higher E_{ox} stress values. This is a strong indication that the creation of new interface states dominates the trap kinetics at low oxide fields.

On the other hand, at higher stressing field (E_{ox} >2.0 MV/cm) ΔV_{FB} becomes positive thus indicating the accumulation of negative charge in the oxide. As an example, the *C-V* curves at E_{ox} =3.0 MV/cm are shown in Fig. 8. This result is consistent with previously reported data on various gate stack combinations on Si or Ge substrates [9,14]. Also it is consistent with electron trapping from the *n*-Ge substrate. It is interesting to note though, that in the accumulation region the *ΔV* shift (the index *FB* does not apply in this case) is more pronounced than the ΔV_{FB} change in the depletion region. It is also more pronounced than the simple "stretch-out" effect we observed at low E_{ox} values (Fig. 5) and could be attributed to the high density of bulk oxide defects. A possible explanation for the positive ΔV_{FB} shift is the following.

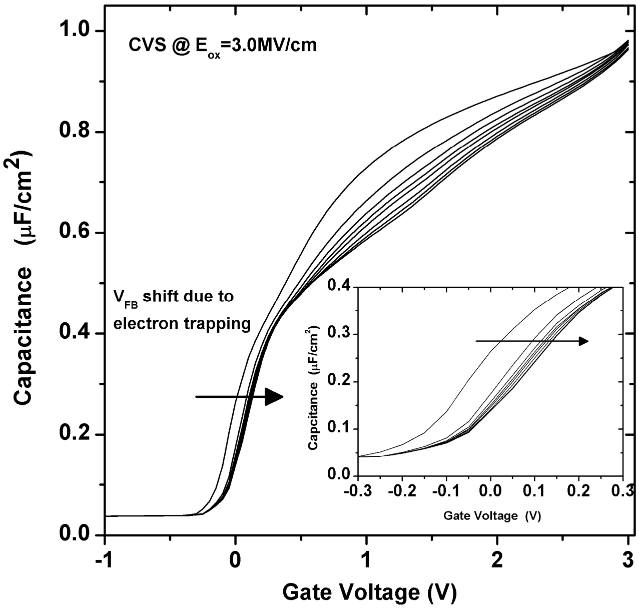


Fig. 8. *High frequency C-V curves (f=100KHz) measured after CVS at a corresponding* E_{ox} *= 3 MV/cm. Positive shift of* V_{FB} *with stress time is observed as indicated by the relevant arrow. And the insert displays an enlarged view of the curve around* V_{FB}.

At low stress field values the total trap density (neutral or charged) in the dielectric (CeO_2) remain constant whereas the stress induced flatband shifts, are mainly due to creation of new interfacial defects, as well as, trapping of holes on the pre-existing interface traps. At higher fields, the bulk oxide traps are involved in the process together with the creation of new bulk traps, which must be also taken into consideration. The dependence of the voltage shift (ΔV_{FB}) on stressing time (*t*) can be expressed as [8]

$$\Delta V_{FB} = \Delta V_{\max}\{1 - \exp[-(t/\tau)^{\gamma}]\} \tag{3.2}$$

where ΔV_{max} is the maximum voltage shift, and τ is the time constant of the process, which is defined as[12]

$$\tau = \frac{q}{\sigma_i J_g} \tag{3.3}$$

where q is the electron charge, σ_i is a characteristic capture cross section for the ensemble of traps with a continuous distribution of cross sections, γ is an exponent which characterizes the distribution in capture cross sections and J_g is the mean current density injected into the dielectric during the electric field stress. Therefore, an equivalent approach to Eq. (3.2) is to describe the change of ΔV_{FB} as a function of the injected charge (Q_{inj}) as:

$$\Delta V_{FB} = \Delta V_{\max}\{1 - \exp[-(\frac{\sigma_i Q_{inj}}{q})^{\gamma}]\} \tag{3.4}$$

here ΔV_{max} is related to the total oxide trap density. Exponent γ is a measure of the distribution width and its value increases to 1 as the distribution width decreases to zero. The injected charge is calculated from the fundamental equation:

$$Q_{inj} = \int_0^t J_g(t)\,dt \tag{3.5}$$

In this case the evolution of charge trapping with time is transformed to the dependence of the trapped charge as a function of the injected into the oxide charge from the semiconductor substrate. From J_g vs t measurements during CVS (not shown here for clarity) it was clear that the stress induced leakage currents (SILC) were very small, thus the J_g current was almost constant during the stress time intervals used in our experiments (t= 500s or 1000s) so, Eq. (3.5) reduces to the simple form: $Q_{inj} = J_g t$.

The result of various stress fields on the ΔV_{FB} shift is illustrated in Fig. 9, where the negative shift at low E_{ox} values is clearly observed. The inset in Fig. 9 shows an enlarged picture of the same curve for E_{ox}= 2MV/cm in a log-log plot. The straight line that fits to the experimental data shows that the ΔV_{FB} shift follows a power law expression with respect to Q_{inj} which is given by [3]

$$\Delta V_{FB} = BQ_{inj}^{m} \tag{3.6}$$

The calculated value for $m=0.77$, lies in the range [0.3 –1.0] as reported by many groups in the past irrespective of the substrate material chosen (Si or Ge) [14-17]. This behavior has also been observed on similar structures [9,12,14-16] and is in general, attributed to the creation of new traps. Therefore, it is also consistent with the corresponding *C-V* and *G-V* curves (Fig. 5 and Fig. 6), which show an additional contribution from these interface states.

However, when the stress field (E_{ox}) is higher than 2MV/cm the situation is different. As shown in Fig. 9 ΔV_{FB} shifts are positive and they follow the exponential form of Eq. (3.4). The corresponding σ_i values are 1.3×10^{-19} cm^2 and 0.6×10^{-19} cm^2 for E_{ox} = 3MV/cm and 4MV/cm respectively. It is interesting to notice that for both fields the experimental data are perfectly fitted by Eq. (3.4) with $\gamma\approx1$. In this case Eq. (3.4) describes the filling dynamics of pre-existing bulk oxide traps with no continuous distribution in its capture cross section. From the small values for the capture cross section it is inferred that the traps are neutral [18]. In addition, the decrease of σ_i with increasing stress field has been observed in neutral and coulombic centers in SiO_2, HfO_2 and Al_2O_3 in the past [8-9].

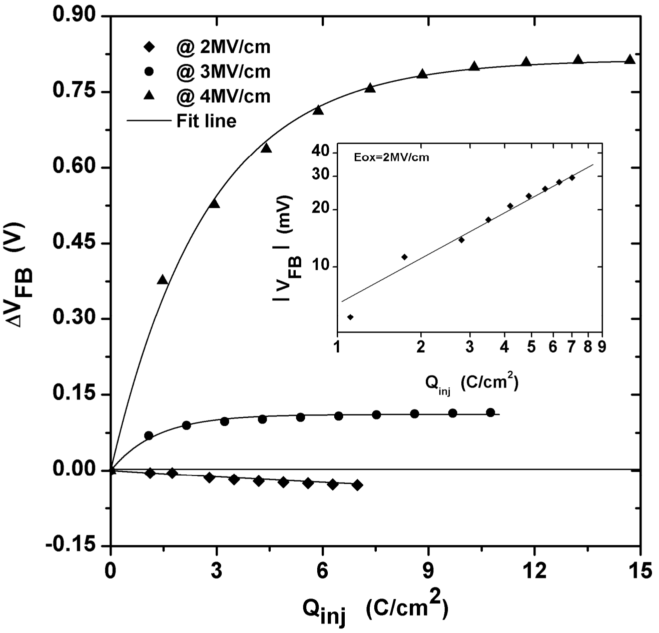


Fig.9. *Charge trapping monitored by flatband-voltage shift ΔV_{FB} of Pt/CeO$_2$/n-Ge as a function of injected fluence under various stress electric fields. Solid lines are best fit to experimental data according to Eq. (3.4) and Eq. (3.6).*

Therefore, we could argue that low stressing field (2MV/cm) results in the creation of new interfacial defects thus distorting the corresponding *C-V* curves. When the capacitance at flat-band condition is monitored it seems to shift towards more negative V_g values. However, it is the "stretch-out" of the *hf-C-V* that is responsible for this effect. On the contrary, high stressing field (≥3MV/cm) results in a different conduction mechanism through the dielectric. The high density of electrons injected from the Ge substrate tunnel through the oxide defects so, we observe negative charge trapping on these defects. Finally, from the *C-V* measurements, it is inferred that at E_{ox} values as high as 4MV/cm, the amount of new, stress-induced oxide defects is undetectable and probably masked by the stronger electrical effect of charge trapping on the pre-existing bulk oxide defects.

One important issue to understand is to what extent charge trapping in rare earth oxides grown on Ge substrates is intrinsic to metal oxides and how can this problem be cured. For example, Gusev *et al.* [19] studied HfO_2 layers deposited on silicon substrates with or without special interface preparation and they found that charge trapping does depend on interface quality. They have also shown that rapid thermal annealing in nitrogen environment is not sufficient to reduce these oxide defects. In a recent work [20] the authors suggest that the preexisting oxygen vacancies in HfO_2 based *n*-type MOS field-effect transistor can be cured by proper post deposition annealing (re-oxidation under proper conditions). Our results are in agreement with the above-mentioned studies, i.e., oxygen vacancies in rare earth oxides grown on Ge play a very important role in the charge trapping dynamics of the corresponding systems. The choice of different semiconductor substrates (Ge instead of Si) is not so important. It is the semiconductor/insulator interface quality that makes the difference. However, the common post-deposition annealing process for Si based devices in hydrogen (FGA) is not sufficient for the similar Ge based structures.

B. Correlation of Charge Build-up and SILC in CeO_2 films

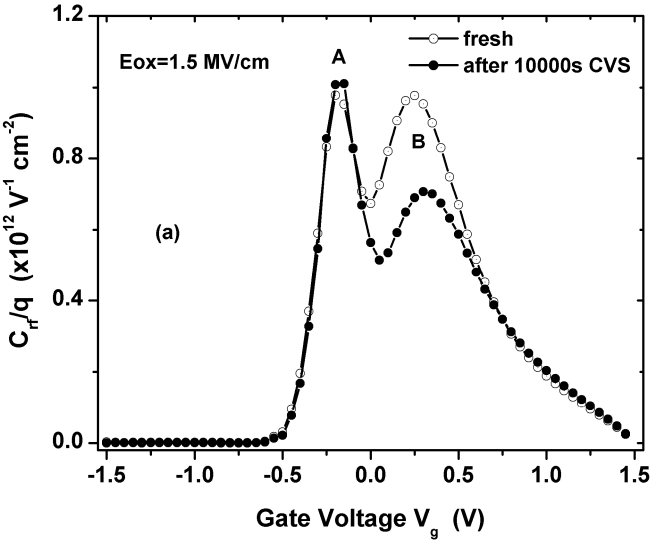
3.4 Results and Discussion

An overview of this section is as follows. *First*, we show that an analysis of the high frequency (*hf*) C-V_g hysteresis loops gives a rather clear indication for the evolution of both interface and bulk oxide defects. *Second*, we examine the gate current, whose increase with time during moderate field stressing suggests the build-up of negative charge together with the creation of new defects in the dielectric. *Third*, we study the evolution of the gate current after the application of a low forward CVS bias where relaxation effects are present. *Fourth,* we investigate the change of both the build-up charges and SILC coefficients with the applied forward stress, in order to estimate whether the reliability results obtained after CVS at higher fields can be extrapolated at typical MOS operating fields. *Finally*, we calculate and discuss the capture cross section of investigated traps.

3.4.1 Change of "Border Traps" with Stress

In a pioneering paper, Fleetwood et al. [21] introduced the concept of "border traps" as a new sub-class of defects commonly appearing in MOS devices. These defects lie physically within the oxide but are near enough to the semiconductor/oxide interface and they often act indistinguishably from interface traps. In electrical measurements at a given effective frequency, interface traps and border traps close enough to the interface and/or at appropriate energies can change charge states (for example, during a C-V_g or I_g-V_g ramp) if they can communicate with the semiconductor (Ge in this case) on time scales faster than the characteristic measurement times. Bulk oxide traps which do not communicate with the Ge on the measurement time scale are considered here as bulk oxide states following the common nomenclature of electrical characterisation of MOS devices.

One measure of the effective border trap densities can be obtained from C–V_g hysteresis [21]. It is rather obvious that the slower the ramp rate, the more border traps can exchange charge with the Ge substrate. Here a ramp rate of ~0.1 V/s was used, corresponding to switching times of ~40 s over the portion of the curve showing



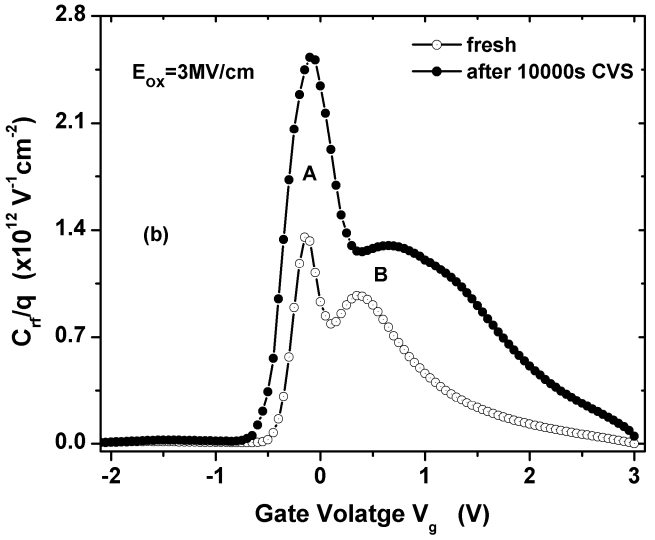


Fig. 10. *Border traps density per unit energy (C_{rf}/q) vs. gate voltage V_g for the case of: (a) low applied field across the oxide (E_{ox} = 1.5MV/cm) and (b) high field (E_{ox} = 3.0MV/cm). Peak A is mainly due to the interface defects while peak B is attributed to bulk oxide defects only.*

hysteresis. Border traps with switching times slower than this will be counted as bulk trapped charges in these measurements, and those with switching times comparable to that of interface traps (~1ms or less) will be counted as interface traps.

However, a better measure of the effective border trap density, ΔN_{bt}, can be obtained by integrating the absolute value of the difference between the high frequency C-V_g curves; that is

$$\Delta N_{bt} \approx \frac{1}{qA}\int \left|C_r - C_f\right| dV \qquad (3.7)$$

The C–V_g difference curve, $C_{rf}(V_g) = (C_r - C_f)$, is a function of the applied gate voltage. The indexes refer to measurement from accumulation to inversion ($C_r = C_{\mathrm{reverse}}$) and inversion to accumulation ($C_f = C_{\mathrm{forward}}$) respectively. Experimental data of $C_{rf}(V_g)$ curves are shown in Fig. 10 for different stress voltages always at accumulation. Only the curve before stress and the last one (after ten stress cycles) are shown for clarity. Usually they are strongly peaked functions, going to zero above flatband or below inversion. In the data shown in Fig. 10 though, one peak lies in the depletion region (peak A) where mainly the interface traps respond, while another peak (peak B) in strong accumulation appears in all curves. The deformation of the C-V_g curves in accumulation is commonly attributed to excess charge trapping in the oxide and is usually absent in state-of-art, Si-based MOS devices. However, even in the case of a strongly peaked $C_{rf}(V_g)$ function at depletion, this peak is due to both interface and bulk oxide traps. Therefore, the curves in Fig. 10 were deconvoluted in order to study separately the two kinds of traps. As illustrated in Fig. 10(a), peak A remains constant after CVS at low applied fields and a total stress time of 10000s, while peak B decreases. The result is reasonable for the peak due to the interface states; their density does not change after CVS at low fields. The reduction of peak B though, could be attributed to the capture of positive charges but this is impossible as the MOS devices are biased in accumulation and the Ge substrate is n-type. The picture is completely different in Fig. 10(b) where the applied stress field is moderate (3MV/cm); both peaks increase mainly because of the creation of new (interface and bulk) defects. Therefore it is reasonable to assume that the reduction of peak B in Fig. 10(a) is due to the presence of relaxation effects in the oxide. This assumption is supported also from other measurements as will be explained in the next paragraphs.

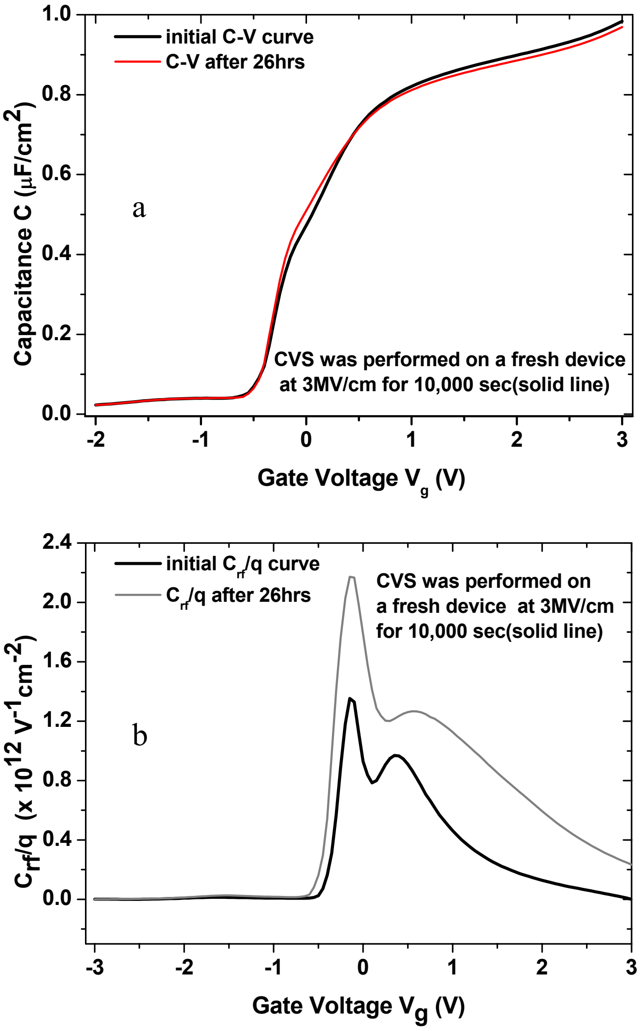


Fig. 11: (a) *C-V* cureves before stressing at 3MV/cm for 1000s and 26hours after end of the stress and (b) corresponding “Border traps” analysis.

Some remarks must be made about the measurement procedure (see Fig. 10 and the relevant text in the previous section) and the interpretation of the data obtained in this way. It is well-known that trapping is a strong function of the applied field and that this can be understood as the result of equilibrium between trapping/detrapping processes in the oxide. Moreover, when the stress is stopped, a redistribution of charges in the oxide is observed [22]. In this way, the trapped charge density measured during the monitor ramps cannot be considered as a direct measure neither of the trapped charge density during the high-field stress conditions nor of the generated trap density. Only an effective trap density is measured which corresponds to the traps which are filled under the monitor conditions.

The C-V curves before stressing one diode at 3MV/cm and 26 hours after the end of this stress cycle (total time 10000 sec at 3MV/cm) are shown in Fig. 11(a). We believe that there is a clear indication of an additional amount of "new" interface-like defects in depletion. Moreover, in Fig 11(b), a comparison of the corresponding "border-traps" curve is presented where it is clear that the change in $C_{rf}\,(V_g)$ though the MOS capacitor was not under bias.

3.4.2 . CVS at moderate E_{ox}

The effective dielectric constant of the polycrystalline CeO_2 thin films was evaluated from the high frequency (f=100 kHz) Capacitance-Voltage (C-V_g) characteristics of the MOS devices and was found to be around 25 in agreement with previously reported data on similar structures [23], [24]. Although the dielectric constant is quite high, the corresponding devices are rather leaky due to the low band gap of CeO_2 (~3.3eV) in tandem with the small conduction band offset [25]. The current transport mechanism of the studied MOS devices is illustrated in Fig. 11. Due to the small conduction band offset the leakage current in accumulation mode is because of thermionic (Schottky) emission at low to medium fields across the dielectric layer [26]. At higher fields though, it is the Poole-Frenkel emission that controls the conduction through the oxide. The results shown in Fig. 11 have been confirmed also in a series of similar structures with CeO_2 thicknesses ranging from 6nm to 9nm with temperature dependent I_g-V_g measurements [27].

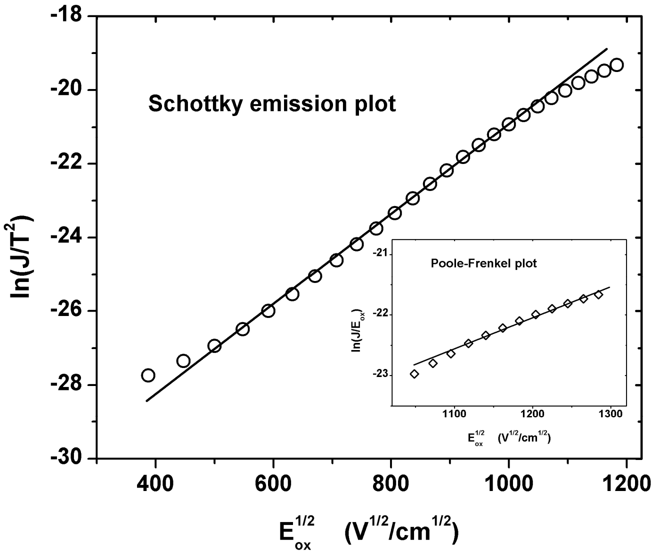


Fig. 12 *Typical J-E_{ox} curve of the devices showing Thermionic (Schottky) emission at low to moderate E_{ox} values. The insert shows a Poole-Frenkel plot as this mechanism dominates at higher E_{ox} values.*

Fig. 13 and Fig. 14 show the current density change (ΔJ) during the application of a CVS pulse. The experimental data can be very nicely described by a model proposed by Nigam *et al.* [28] where ΔJ as a function of time (t) is given by the following equation:

$$\Delta J = N^{+}(E_{ox}) \cdot \left[1 - e^{-\frac{t}{\tau}} \right] + \alpha \cdot t^{\nu} \tag{3.8}$$

with $N^{+}(E_{ox})$ being the saturation value of positive charge trapping, τ the trapping time constant and α and ν the SILC related parameters, as discussed further on. The first term in the (3.8) represents an exponentially saturating trapping of negative charges on pre-existing oxide defects, while the second term represents the increase due to SILC-generation.

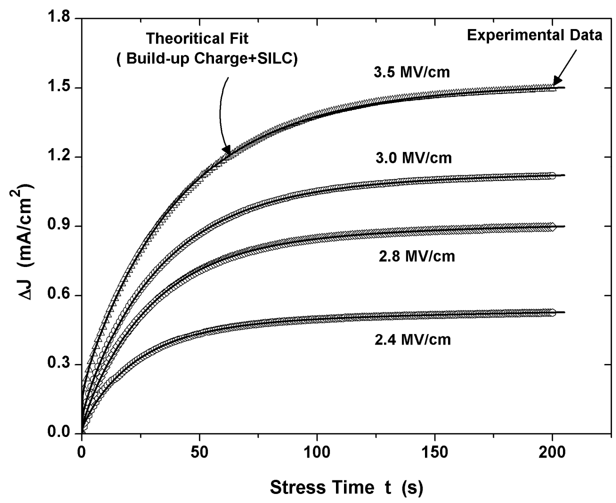


Fig. 13. *Change of current density ΔJ observed during the stress time t under moderate to high stress field (CVS conditions). Symbols are experimental data, while solid lines are best fit of both SILC and charge build-up according to (3.9).*

One difficult task in obtaining the necessary ΔJ ($=J-J_o$) values from the experimental (J,t) pairs is the determination of the first value of current density J_o. This value is actually equal to the leakage current of the device when no stress is applied. Small changes of J_o lead to a complete different slope of the curve and, therefore, an uncertainty in the fitting results, proving the necessity to determine J_o more accurately [29]. Fitting the actual current instead of current change and treating J_o as a fit parameter can overcome this problem. In other words the (3.8) is rewritten as:

$$J = J_o + N^{+}(E_{ox}) \cdot \left[1 - e^{-\frac{t}{\tau}}\right] + \alpha \cdot t^{\nu} \tag{3.9}$$

Fig. 13 shows the absolute value of the measured current $|\Delta J|$ in the electric field E_{ox} range 2.4 MV/cm up to 3.5 MV versus time on a linear scale. The full line indicates the fit with (3.9). It should be noted here that, although the actual experimental data

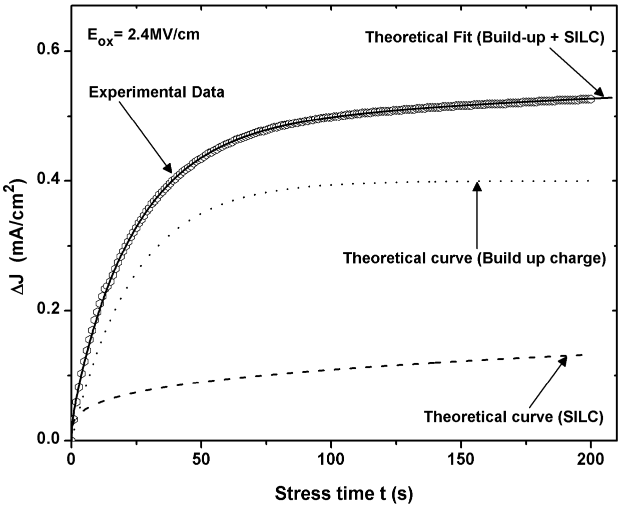


Fig. 14: *Contribution of charge build-up (dotted line) and SILC (dashed line) to the total ΔJ vs t experimental curve (symbols) at 2.4MV/cm. The solid line represents the summation of the two terms (SILC and Charge build-up) according to (3.9).*

were fitted with (3.9), in Fig. 4 ΔJ vs t curves are illustrated as it is easier to study the trapping and SILC mechanisms with increasing applied stress field. The contribution of the two terms is illustrated in Fig. 14 for the case of applied stress bias E_{ox}= 2.4MV/cm. The charge trapping component (the first term in (3.9)) clearly dominates as SILC is still not significant. Nevertheless, at higher fields the experimental curve never reaches a saturation value because of the SILC component which becomes significant. Similar results have been found in SiO_2/Si based devices [29] showing that the models used to explain oxide degradation are valid also in the case of Ge based MOS devices. The most important difference in the case of a rare earth oxide is that the charge trapping component dominates over SILC in the entire field range (for applied stress fields from around 1.8MV/cm up to 4.0MV/cm).

However, when intermediate or very low electric fields (from 0.5MV/cm up to 1.6MV/cm) were applied during the CVS measurements, the results were rather complicated as will be discussed in the next paragraph.

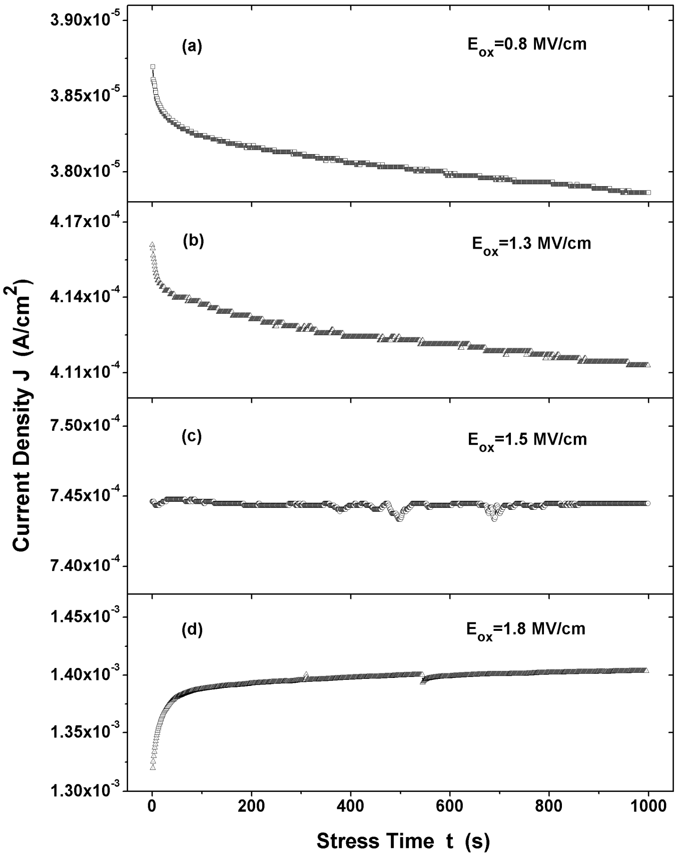


Fig. 15: *Current density J as function of stress time t during CVS at lower stress field (0.8 MV/cm up to 1.8 MV/cm), showing relaxation effects for applied* E_{ox}< *1.3MV/cm.*

3.4.3 CVS at low E_{ox}

Fig. 15 (a)-(d) shows a set of *ΔJ,t* curves for CVS conditions at E_{ox} = 0.8 , 1.3, 1.5, and 1.8 MV/cm respectively. It is interesting to notice that, at very low fields, CVS results in decreasing gate currents (Fig. 15(a) and (b)). As there is no apparent source of positive charges when the n-Ge MOS devices are biased in accumulation, the realistic explanation is the presence of relaxation effects. These effects are expected to be detected in high-*κ* films when the leakage current is low. Therefore, a typical method for the estimation of the relaxation currents is to be measured after the sudden removal of a constant voltage on the gate [30]. However, this study was focused on the investigation of charge trapping mechanisms and such a measurement was not done. This is the reason that the relaxation effects are so weak in Fig. 15(a) and (b) and no attempt was made to fit the experimental data with the Curie–von Schweidler law (*J~1/t*). Nevertheless, the effects were studied more carefully in similar devices and results on Pt/HfO_2/Dy_2O_3/Ge devices have already been recently reported [31].

At these low fields and at room temperature conditions, SILC effects are negligible and an enormous amount of time is needed before a change in J can be observed. For example, it has been shown by Stathis *et al.* [32] that, for an oxide with this thickness and area of 5×10^{-4} cm^2, it takes approximately 300 years to reach breakdown at $|V_g|$=1.9 V. In this case, therefore, it is impossible to reach breakdown at lower fields within a reasonable measurement time.

However, when the applied fields are greater than 1.8 MV/cm approximately, the current through the oxide is at least one order of magnitude greater and the current transport mechanism changes from Thermionic emission to Poole-Frenkel (Fig. 12) so, that the high density of bulk oxide defects are responsible for the leakage current thus masking all relaxation effects.

Finally, at applied fields between these two extremes (that is from 1.3MV/cm up to 1.6MV/cm) the corresponding *J-t* curves are almost flat over the entire time interval, as none of the above mentioned effects clearly prevails.

3.4.4 The build-up charges and SILC coefficients

Fig. 16 and Fig.17 show the fit parameters of (3.9) as a function of the applied electric field. The parameters in Fig. 16 are related to the negative charge trapping behavior of the oxide. As shown in the figure, the trapping time constant (τ) increases linearly with increasing applied field. Similar to the observations of Nigam *et al.* [28] and Xie *et al.* [33] on SiO_2/Si structures it is the considerably smaller number of available oxide traps that makes the trapping time constant longer at lower fields.

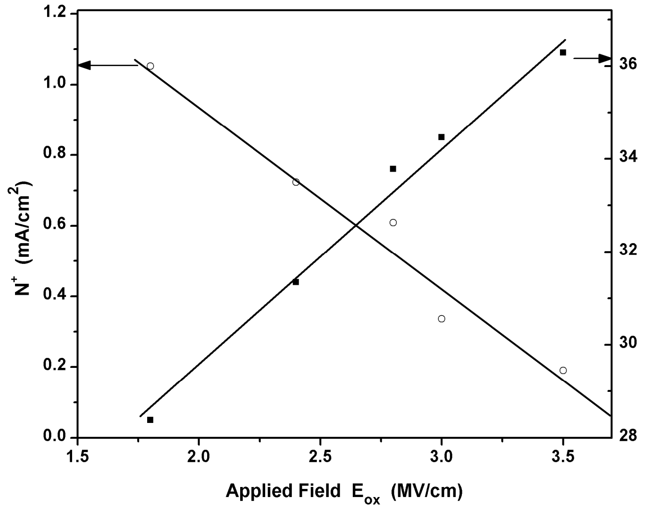


Fig. 16. *The fit parameters N^+ (left axis) and τ (right axis) related to the charge build-up term as a function of E_{ox}. The lines are simply guide to the eye.*

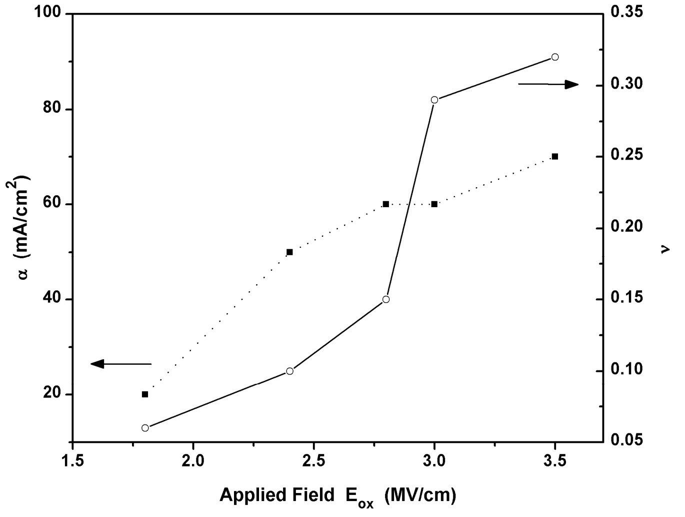


Fig. 17: *The fit parameters leakage current α (left axis) and trap generation rate v (right axis) related to the stress induced leakage current (SILC) as a function of* E_{ox}*. The lines are simply guide to the eye.*

The corresponding τ values (~30sec) indicate neutral defects as will be discussed later. At the same time, N^+ decreases with respect to the applied stress bias, which indicates that charge trapping becomes less important at higher fields. Another important observation is that the pre-exponential factor N^+ is almost six orders of magnitude greater than conventional Si/SiO$_2$ based devices [29]. This is probably due to the poor interfacial germanate layer, which is not eliminated after the conventional FGA treatment used in the present study.

In Fig. 17, the SILC-related parameters are plotted against the applied stress bias. Since SILC is directly related to the trap generation in the oxide, especially at low injected fluence, both α and v provide information on the stress-induced trap generation [28]. α is the leakage current caused by the traps generated after t=1 second and v is the trap generation rate. Both parameters (α and v) increase with increasing field showing that SILC becomes important at higher stress fields, as a consequence of the trap generation density dependence on the field stress applied during oxide degradation. Similar results have been reported on Si based MOS devices with different dielectrics such as: v=0.15 to 0.30 on SiO_2/Si [28], [34], [29] and v=0.73 on HfO_2/Si [35]. The calculated v values for a CeO_2/Ge system indicate that the choice of semiconductor substrate plays no important role in the mechanisms involved in SILC creation.

3.4.5 Capture cross section of traps investigated

The trapping time constant (τ) used in (3.9) is given by [12]

$$\tau = \frac{1}{\overline{\upsilon}\sigma_t n_e} = \frac{q}{\sigma_t J_g} \tag{3.10}$$

where $\overline{\upsilon}$ is the mean thermal velocity of electrons in CeO_2 which is considered approximately equal to the electron drift velocity, q is the electronic charge, n_e is the average injected electron density and J_g the mean current density injected into the gate dielectric during the electrical stress, which is approximately proportional to n_e. The cross section of the traps (σ_t) is defined as the ratio of the capture probability to the thermal velocity of the electrons.

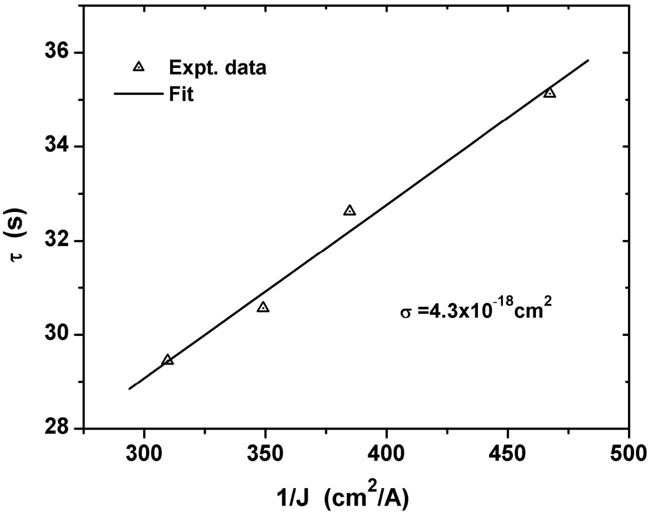


Fig. 18: Time constant τ as a function of inverse current density (1/J) injected into the gate dielectric during constant voltage stress (CVS) at moderate stress fields. The capture cross section is obtained from the slope of the best fit line according to (3.10).

The time constant τ was extracted from the experimental curves shown in Fig. 5 and Fig. 15 using (3.9) and is plotted in Fig. 18 as a function of $1/J_g$. It is observed that τ varies almost linearly with $1/ J_g$, as predicted by (3.10), hence the trap cross section σ_t was estimated from these data to be around 4.3×10^{-18} cm^2. Quite small values for σ_t have been also found in similar high permittivity gate stacks grown on silicon (Si) substrates as compared to values of the order of 1×10^{-16} cm^2 in SiO_2. These small values for the capture cross section suggest that the traps generated during the electrical stress are neutral centres [36-37]. In the case of SiO_2, neutral trapping centres with cross section on the order of 10^{-16} cm^2 have been attributed [38] to SiOH centers generated during the release of H^+ by hot electron impact ionization at the anode, followed by the breaking of bridging O bonds by these H^+ protons, which are subsequently trapped by the resulting SiO_2 sites. In the present case though, this mechanism is not likely to happen as the applied fields are not strong enough to create hot electrons.

3.5 Summaries

In this chapter, charge trapping phenomena were studied in Ge based MOS structures with CeO_2 as the dielectric layer. All devices were initially annealed in forming gas at 200 °C in order to improve slightly their electrical characteristics. The investigation of the trapping characteristics of the cerium oxide dielectric layer by means of analysis of the relevant flatband shift of the hf *C-V* curves could only provide information for the preexisting bulk defects. CeO_2 dielectrics were subjected to constant voltage electrical stress in order to study some fundamental reliability issues of the corresponding devices. For stress fields higher than 1.8 MV/cm it was observed that the contribution of the charge trapping component has a significant impact on the measured curves while the effect of SILC component is faint. In the applied field range studied (1.8MV/cm up to 3.5 MV/cm) SILC generation follows a power law model similar to a number of works reported earlier on SiO_2/Si structures. The trap generation rate was found to be very small but rapidly increasing with increasing stress bias. These results are not surprising since the high-κ dielectrics currently studied are good insulators and suffer from the high density of both interfacial and bulk defects. Direct comparison of the N^+ and ν values of the MOS capacitors studied in the present work to SiO_2/Si based systems is rather useless as the latter suffer from SILC generation due to tunneling currents while trapping on preexisting defects is very small. The effective cross section of the traps obtained from the analysis of the *J-t* curves was very small ($\sim 10^{-18}$ cm^2) suggesting the presence of neutral traps. As the post annealing treatment in hydrogen environment (FGA) did not result in better (in terms of leakage current) devices, one can conclude that the main type of defects is oxygen vacancies, a common problem in high-k dielectrics. Finally, a very weak relaxation effect was detected at applied stress fields lower than 1.8 MV/cm.

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Chapter 4

"Current Transport Mechanism in High-κ Cerium Oxide Gate Dielectrics Grown on Germanium (Ge)"

4.1 Motivation

The current transport mechanism of Pt/CeO_2/p-Ge MOS devices is investigated. The results are based on the analyses of gate current vs gate voltage curves at temperatures ranging from 295K to 375K. We observe two different current conduction mechanisms at different applied fields. At low to medium electric fields (~0.1-0.9 MV/cm) the main current conduction mechanism is Schottky emission while Poole-Frankel conduction is the dominant mechanism at higher fields across the oxide (~1.2-2.1 MV/cm).

4.2 Introduction

High-κ dielectrics as an alternative to conventional SiO_2 gate oxides are widely investigated for their capability to reduce excessive leakage current in future complementary-Metal-Oxide-Semiconductor (CMOS) devices. Although their functionality is already proven and the first integrated devices are in production, further scaling becomes increasingly difficult. Hence, Ge which offers higher electron and hole mobility than Si is currently considered as a potential alternative to the standard Si-based MOS technology because, it might increase the high frequency performance of logic devices keeping at the same time the power consumption low.[1] Among the high-κ dielectrics being studied, rare earth oxides (REOs) are widely investigated because of their interesting structural and electrical properties as a buffer layer on

Ge substrates.[2] REOs offer good passivation of Ge, thus reducing the density of interface states (D_{it}), they have reasonably high dielectric constants and some of them are good insulators with energy bandgap greater than 5.0 eV.[3-4] In particular, cerium oxide (CeO_2) seems to be an interesting dielectric because, it can be deposited directly on Ge with good thermal stability and improved electrical characteristics such as, high dielectric constant (κ~23) [3] and low interface traps density (D_{it}~5×10^{11}eV/cm^2).[2,5] The moderate band gap (3.3eV) [6] together with the small conduction band offset [4] lead to relatively high leakage currents (~10^{-4} A/cm^2) [2,4,7] which is a serious drawback if the material is to be used alone and not in a gate stack configuration.[8]

Recently, *Fu-Chien Chiu*, reported on the current conduction mechanisms of CeO_2 deposited on Si(100) wafers with Al as the gate electrode.[9] The author found that Schottky emission is the dominant conduction mechanism in a medium electric field while Poole-Frenkel emission prevails at higher electric fields and higher temperatures (up to 500K). In this chapter, we report on the temperature dependent carrier transport mechanism of thin (~7nm) CeO_2 films grown by Molecular Beam Deposition (MBD), and the related energy bang diagram of Pt/CeO_2/p-Ge structures.

4.3 Experimental

The CeO_2 films studied in the present work were prepared by MBD on p-type (001) Ge substrates with resistivity 1.6-1.9 Ω-cm. The oxide was deposited at 225^{o}C by evaporating Ce metal in the presence of atomic oxygen beams, generated by an RF plasma source. MIS capacitors with area A=7×10^{-4}cm^2 were defined by e-beam evaporation of 30-nm-thick Pt, using a shadow mask to define circular dots 300 μm in diameter. The thickness of the samples was estimated by X-Ray reflectivity measurements to be 7nm approximately. The electrical properties *C-V* and *I-V* curves were measured at different temperatures by means of an Agilent 4284A LCR meter and a Keithley 617 electrometer.

4.4 Results and Discussion

The effective dielectric constant of the polycrystalline CeO_2 thin films was evaluated from the high frequency (f=100kHz) Capacitance-Voltage (*C-V*) characteristics of the MOS devices and was found to be 25.5 in accumulation mode. Therefore, an EOT of about 16.2Å was estimated taking into account quantum effects. At RT the relevant *C-V* curve indicates the presence of the so called "slow states", while at higher temperatures they show dispersion at depletion and inversion. The effect is well known from Si based devices but is more significant when Ge is used as the substrate due to its smaller bandgap [10]. The D_{it} value at midgap calculated from the *C-V* curves at RT was around 1×10^{12} $eV^{-1}cm^{-2}$. As this value probably overestimates the true density of interface states,[10] it is also in agreement with best results reported on similar devices with REOs as gate dielectrics.[2,4]

In order to understand the carrier transportation mechanisms of the CeO_2 dielectric, the temperature dependence of the gate leakage current density (J_g) was investigated at the same temperature range (295–375K), both under gate and substrate injection. As illustrated in Fig.1, typical current densities at 295K were about 0.4 mA/cm^2 at V_{FB}-1V in accumulation and slightly higher at inversion. Also the currents (at $V_{FB}\pm1V$) in both forward and reverse gate polarities are of the same order of magnitude, which indicates that the conduction mechanism is a bulk limited [11] process. The rather high J_g values are consistent with the low energy gap of CeO_2 (~3.3 eV) [6] and the inevitably low band offsets.[4,6]

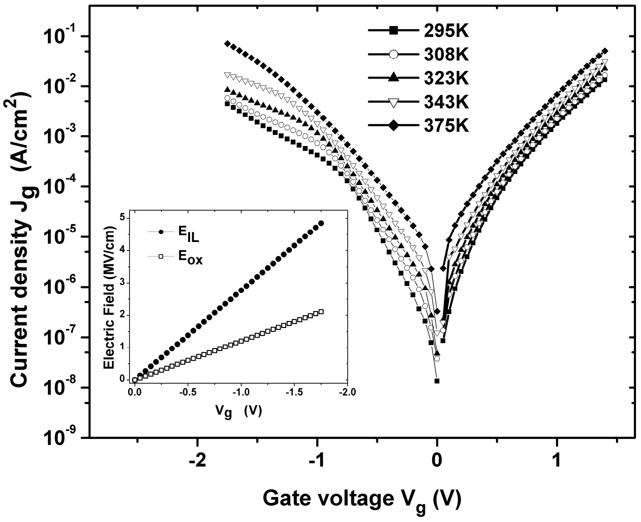

Fig. 1: *Current density J_g as function of the voltage across the gate dielectric (7nmCeO_2) of a Ge-MOS capacitor recorded form 295K to 375K. Insert graph shows electric field in the Ce-O-Ge interfacial layers and CeO_2 layers as a function of applied voltage as calculated from Eqs. (4.1) and (4.2).*

When CeO_2 is deposited on Ge, it reacts with the substrate resulting in catalytic oxidation of Ge and spontaneous formation of a stable and thick Ce-germanate (Ce-O-Ge) interfacial layer(IL).[4] Assuming that no charge is accumulated at the CeO_2/germanate interface, the electric field across the two layers (IL and CeO_2) is given by [12]

$$E_{IL} = \frac{V_{applied}}{(\kappa_{IL} / \kappa_{ox})t_{ox} + t_{IL}} \tag{4.1}$$

$$E_{ox} = \frac{V_{applied}}{(\kappa_{ox} / \kappa_{IL})t_{IL} + t_{ox}} \tag{4.2}$$

where $V_{applied} = V_g - V_{FB}$ is the voltage applied to the gate dielectric stack, V_{FB} is the flatband voltage. The dielectric constant of the interfacial layer (κ_{IL} =11) [8] has been measured separately using a set of similarly grown MOS devices with different CeO_2 thickness (from 8 to 17nm), while κ_{ox} =25.5 was assumed for the CeO_2 layer, t_{IL}=1nm and t_{ox}=6nm are the relevant physical thicknesses as obtained from TEM [4] measurements. The electric field across each layer as calculated from Eqs. (4.1) and (4.2) is shown in the insert of Fig.1.

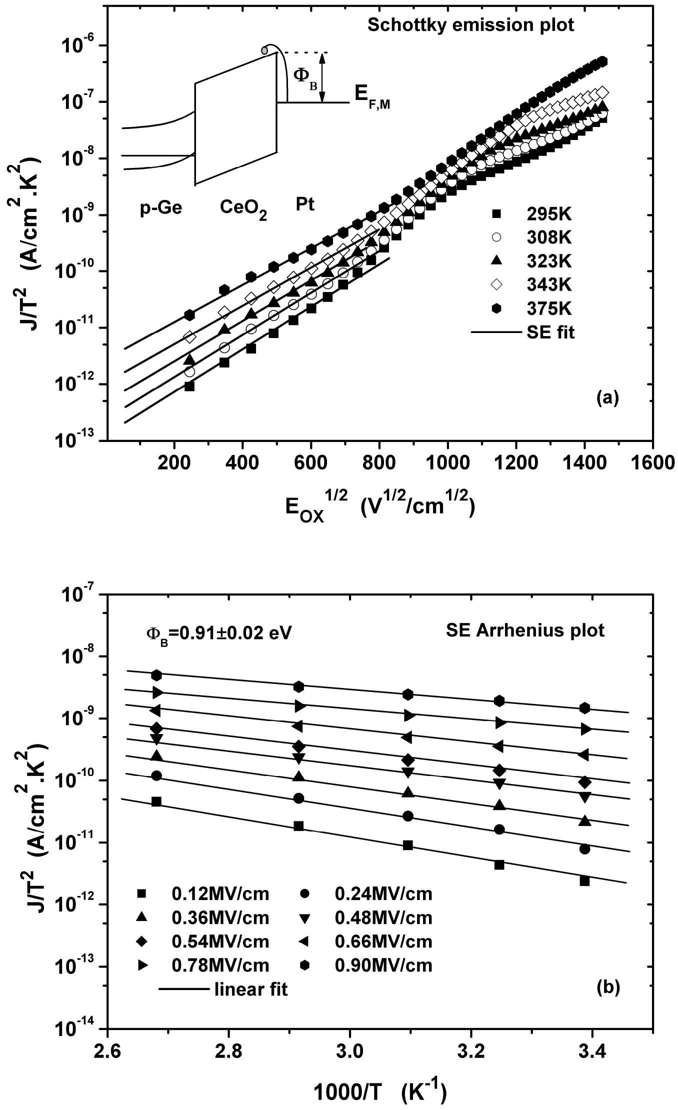

Fig. 2: *Schottky emission plots in the temperature range 295K to 375K and low applied field under gate injection. The Pt/CeO_2/Ge band diagram is drawn as an insert in Fig.2a.*

Two of the most frequently encountered current transport mechanisms for thin REOs films are the so called Schottky and Poole-Frenkel emissions. After analyzing our data, Space Charge Limited Currents (SCLC) as well as direct or Fowler-Nordheim tunneling currents have been excluded as the main leakage mechanisms due to the strong temperature dependence in the whole gate voltage range. Schottky emission (SE) can be expressed as [13]

$$J_{SE} = A^{*}T^{2}\exp\left[\frac{-q\left(\phi_b - \sqrt{qE_{ox}/4\pi\kappa_d\varepsilon_o}\right)}{k_b T}\right] \tag{4.3}$$

where J_{SE} is the leakage current density, A^{*}(=143 A/cm^2 K^2) is the effective Richardson constant [14] for Ge (100), T the absolute temperature, E the electric field across the oxide, q the electronic charge, $\Phi_b(= q\phi_b)$ the Schottky barrier height, ε_o the free space permittivity, κ_d the dynamic dielectric constant (i.e. the electronic component of the dielectric constant), and k_b is the Boltzmann constant.

The Pool-Frenkel (P-F) conduction mechanism is defined by the following field (E) dependence of the current density $J_{P\text{-}F}$ [13]

$$J_{P-F} = C_t E\exp\left[\frac{-q\left(\phi_t - \sqrt{qE_{ox}/\pi\kappa_d\varepsilon_o}\right)}{k_b T}\right] \tag{4.4}$$

where C_t is a constant proportional to the density of bulk oxide traps, $\Phi_t\ (= q\phi_t)$ is the depth of the trap's potential well, and other terms are as mentioned above.

For standard Schottky emission, a plot of log(J/T^2) versus $\sqrt{E_{ox}}$ should be linear. The dynamic dielectric constant is determined from the slope of the straight lines in these plots and it should be equal to the optical dielectric constant κ_d i.e. the square of the measured refractive index (n^2=κ_d). In the case of gate injection, the data measured at all temperatures (295K-375K) and low to medium electric field (~0.1-0.9 MV/cm) fit the Schottky emission (Eq. 4.3) very well as shown in Fig.2a. From the linear part of the curves, κ_d was found to lie between 3.4 and 3.9 with an error of ±0.2. There is a systematic increase of κ_d with increasing T but at the same time the experimental error in the obtained values of the slopes is rather high due to the uncertainty in the definition of the linear part of each curve. In the past, many groups have studied the dielectric properties of cerium oxides and they reported κ_d values from around 2.0 up to 5.5. The lowest values were found on Au/CeO$_2$/Au MIM structures by *V. Grosse et al.*,[15] who also claimed that the κ_d values obtained when P-F emission

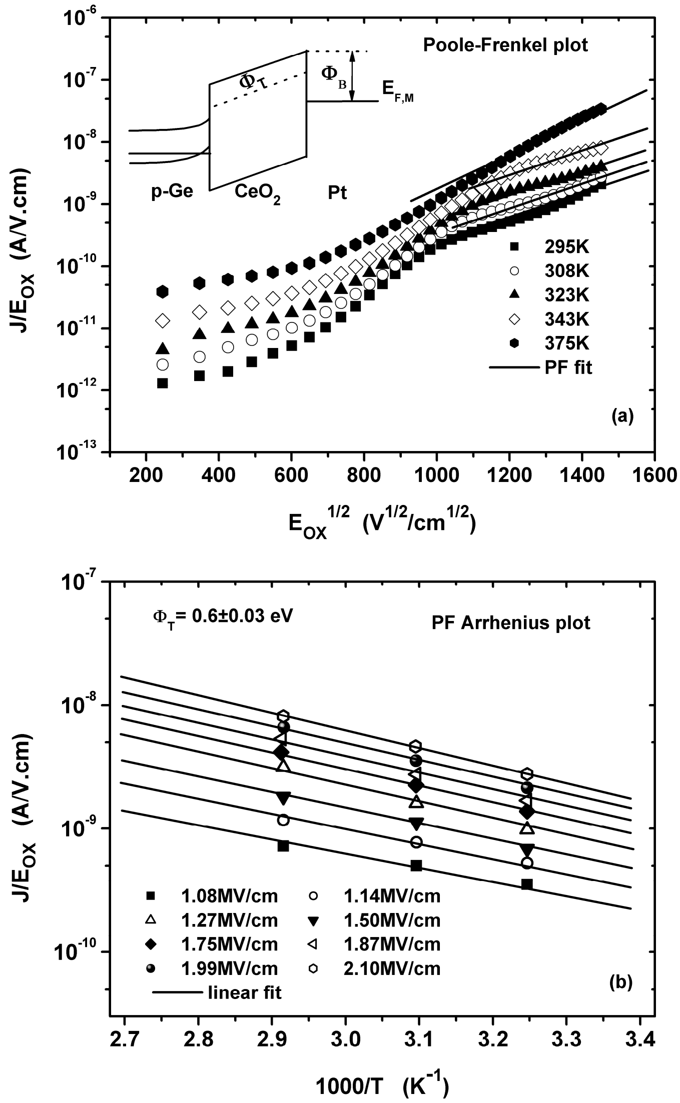

Fig. 3: *Poole-Frenkel (P-F) conduction plots from 295K to 375K under gate injection. The insert in Fig.3a represents the band diagram while Φ_t is the energy level of the traps.*

dominated were significantly lower (1.6 vs 2.3) than in the case of Schottky emission. *Z. Al-Dahhan et al.*[16] have found $\kappa_d = 3.6$ but their structures were too complicated (Al-CeO_2/GeO_2-Al capacitors with thick oxide layers) and their results are under question. In a recent publication *F. C. Chiu* reported κ_d values around 5.5 on Al/CeO_2/Si MOS devices [9] when Schottky emission dominates the current transport. It is interesting to point out here that the corresponding CeO_2 films were grown by RF magnetron sputtering and annealed at 400^oC in N_2 ambient. In addition, the author found similar behavior with respect to the voltage ranges where Schottky emission dominates. Same results have been also shown in Hf-silicate based devices,[17] although the conduction band offsets are quite higher. However, interesting information about the dielectric constant of CeO_2 films comes from an earlier work by *P. Patsalas et al.*,[18-19] where the authors demonstrated a linear dependence of κ_d with respect to its mass density and deposition temperature. This result explains the above mentioned wide spread of κ_d values and is in agreement with the observed wide range ($\kappa_d = 2.1$-3.8) reported on NiSi/Gd_2O_3/p-Si devices.[20] It could also explain the observed increase of κ_d with temperature.

The Schottky barrier height at the Pt/CeO_2 interface was determined to be around 0.91±0.2 eV using a plot of $log(J/T^2)$ as a function of $1/T$, as shown in Fig.2b. In the literature, the Schottky barrier height for Al/CeO_2 is about 0.7eV [21] and 0.9eV [15] for the Au/CeO_2 interface. It has also been reported that, at lower bias voltage range ($\leq \pm 1V$), the dominant current conduction mechanism in CeO_2 is Schottky emission [7, 9, 15, 21].

The Pool-Frenkel emission is presented in Fig.3a, where $log(J/E_{ox})$ is plotted as a function of $\sqrt{E_{ox}}$ for various temperatures. This semi-log plot should be linear if P-F is the dominant conduction mechanism and this is true for the higher E_{ox} values because of the band-bending and tunneling effects. This result is expected and has been reported for CeO_2 and other REO in the past [9, 15, 20-21] The dynamic dielectric constant was obtained from the slope of each P-F plot in Fig. 3a and was found to lie between 3.1 and 3.8 (±1) in good agreement with the values obtained from the analysis of the Schottky plots (Fig.2a). However, it should be noted here that the error in the determination of the κ_d values is slightly higher than in the Schottky case, due to errors in the definition of the appropriate field range where the curves are linear. Moreover, the trap's energy level Φ_t was evaluated using Eq. (4.4) and the slopes of the Arrhenius plots in Fig.3b. Various E_{ox} values have been used and a mean activation energy of $\Phi_t = 0.60 \pm 0.03$ eV was obtained. This level has been plotted in the band diagram of the Pt/CeO_2/p-Ge structure shown as an insert in Fig.3a and is highly probable to be related to oxygen vacancies or divacancies which have been theoretically predicted for a number of high-κ oxides.[22] The obtained Φ_t value is identical to those reported for Al/CeO_2/n-Si structures,[21] where the oxide films were e-beam evaporated and subsequently treated by rapid thermal annealing in N_2 ambient. On the other hand a trap level of 1.12 eV was found in Al/CeO_2/Si MOS devices [9] and a trap with a Φ_t value close to that in thin Gd_2O_3 films.[20] We believe that these results are in agreement with the theoretical work done on HfO_2 and La_2O_3 films,[22] where different charge states of the relaxed oxygen vacancy have been calculated in the forbidden gap of the oxides. Therefore, it is not surprising that different groups report on two defect levels in CeO_2.

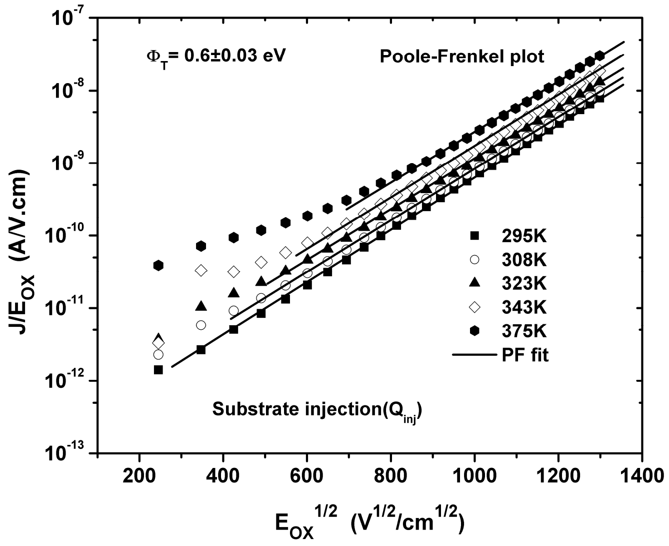

Fig. 5: *P-F plots for various temperatures at accumulation mode (substrate injection (Q_{inj}).*

Finally, the temperature dependence of the current transport mechanisms was studied in inversion mode (i.e. substrate injection). The P-F conduction mechanism was again dominant at higher gate voltages, which explains the similar behavior on both polarities of the J_g-V_g curves (Fig.1). In addition, the obtained Φ_t value was exactly the same as for the accumulation mode as shown in Fig. 4. Furthermore, similar results have been obtained (not shown here for clarity) for other devices grown in the same way but with slightly different thickness of the CeO_2 films (8-10nm).

4.5 Conclusions

In this chapter, the leakage current transport mechanisms of MBD grown CeO_2 films on Ge substrates have been investigated. The electron (Schottky) barrier height at the Pt/CeO_2 interface was found to be equal to Φ_b=0.91eV, while a trap energy level with activation energy Φ_t=0.6eV was detected in the oxide after analyzing the Schottky and Poole-Frenkel emission at lower or higher gate voltages respectively.

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Chapter 5

“Study of Stress Induced Leakage Current (SILC) in HfO2/Dy_2O_3 high-κ gate stacks on Germanium (100)”

5.1 Motivation

In the present chapter, we study reliability issues of Pt/HfO_2/Dy_2O_3/n-Ge MOS structures under various stress conditions. The electrical characteristics of the micro-capacitors are very good probably due to the presence of a rare earth interfacial layer. It is shown that the injected charge (Q_{inj}) at high constant voltage stress (CVS) conditions induces stress induced leakage current (SILC) that obeys a power law. We also observe a correlation between the trapped oxide charge and SILC, which is, at low stress field, charge build-up and no SILC, while at high stress field SILC but few trapped charges. Results show that the present bilayer oxides combination can lead to Ge based MOS devices that show acceptable degradation of electrical properties of MOS structures and improved reliability characteristics.

5.2 Introduction

Dielectrics of higher electric permittivity than SiO_2 (e.g. HfO_2, ~ 25) are investigated widely for their potential use as dielectric layers in advanced Metal-Oxide-Semiconductor (MOS) devices [1-2] aiming to the substantial reduction of gate leakage currents [3]. An important consequence will be the use of thicker (higher permittivity) dielectric layers, and one would also expect to reduce the stress induced leakage current and improve the reliability of the corresponding devices [4]. During the past decade, Germanium (Ge) based MOS devices are extensively studied due to its high mobility [1-2] for the future semiconductor and integrated circuits industry. Nevertheless, not much experimental work has been devoted on the oxide degradation and reliability of high-κ dielectrics for the corresponding MOS devices. Rare Earth Oxides (REOs) are friendly with Ge substrate, so they can be used as an interfacial buffer layer, REOs can also be deposited directly on Ge [5]. The reason is that REOs react strongly with the substrate resulting in catalytic oxidation of Ge and in the spontaneous formation of stable interfacial layers, such as germanate (e.g. La-O-Ge [6], Ce-O-Ge [7]). This germanate layer could be responsible for the reduction of hysteresis and interface state density (D_{it}). Alternative gate dielectric stacks usually consist of an ultra-thin interfacial buffer layer (e.g. Dy_2O_3) and a metal oxide layer with higher electric permittivity (e.g. HfO_2) and a typical thickness of 3-10nm. The gate stack that we are studying is HfO_2/Dy_2O_3 grown on *n*-type Ge with Pt gate electrode. In the present work we have noticed a formation of germanate compound (Dy-Ge-O) at the interface of Ge/Dy_2O_3, which is not shown here.

The first observation of leakage current in thin dielectric layers subjected to high electrical stress field date back to the work of Maserjian and Zamani [8]. This current is commonly termed as stress induced leakage current (SILC) [9]. SILC is one of the main limits in the scaling down of deep submicron technologies; in fact SILC appears long before the occurrence of hard and/or soft breakdown, further reducing the lifetime of devices. Moreover, this SILC hampers the long-term reliability of non-volatile memories, leading to charge loss from the floating gate [10-12] while it can affect dynamic logic and related components. Many papers have been published studying SILC and its relation to device lifetime [8-10]. Quite often accelerated life tests of MOS capacitors are performed by applying a high constant voltage at the gate contact (constant voltage stress, CVS) or by injecting a constant current across the oxide (constant current stress, CCS) over a period of time. The degradation of the oxide is generally monitored by periodically interrupting the stress to allow for electrical measurements, e.g. SILC, flatband voltage shift (V_{FB}), charge trapping, etc. Stress induced leakage current ($J_{SILC} = J_g\text{-}J_0$) is defined as the increase in oxide leakage current density after a high-field stress (J_g), as compared to the leakage prior to any stressing (J_0) [13]. Generation of SILC is also modeled by different studies [8, 12-15].

In the present chapter, we report on the increase in the gate SILC during constant voltage stress [12, 16] of HfO_2/Dy_2O_3 gate stack dielectrics. REOs such as Gd_2O_3, CeO_2, Dy_2O_3, La_2O_3 have been leading candidates in the quest to replace the traditional SiO_2 gate dielectric of MOS transistors with a material having higher dielectric constant (κ=12~23) [6-7,17-19]. REOs can be directly deposited on Ge showing better electrical characteristics than Si with low interface density (D_{it}~10^{12} eV/cm^2 or below) [17-19]. Unfortunately, till now all of the REOs seem to share two deficiencies. First, they cause a SiO_2-like interfacial layer to grow when they are deposited on Silicon (Si) [20]. Second, they also produce electrical instabilities in MOS devices. Electrical instabilities have been the subject of numerous experimental studies [21-27], and it seems possible to interpret many of these as arising from the trapping of charge somewhere with in the gate stack. The SILC variation that we have observed in our study, can not be simply interpreted as a displacement current deriving from charging/discharging of oxide defects close to the interfaces [8]. Charge trapping at the interface between the two dielectric layers of a high-k gate stack is also studied as the two layers have different compositions which means they will have also different conductivities (and transport mechanisms). When the gate bias is applied, the application of a gate bias will immediately produce a discontinuity in current density at the interface between the two layers, causing charge accumulation there until, in steady state, the same current density flows through the both layers. If the gate bias is removed, a discontinuity in current density will again be produced, this time causing the charge to rush out of the gate stack [27, 29].

5.3 Experimental

Dy_2O_3/HfO_2 oxide stacks were prepared by atomic oxygen beam deposition on n-type Ge(100) with resistivity ~0.02 Ω-cm. Native oxide was desorbed in-situ under UHV conditions by heating the substrate to 360°C for 15 minutes, until a (2x1) reconstruction appears in the (RHEED) pattern, indicating a clean (100) surface. Subsequently, the substrate was cooled down to 225°C where the oxide stacks were deposited. The surface was exposed to atomic oxygen beams generated by an RF plasma source with the simultaneous e-beam evaporation of Dy/Hf at a rate of about ~0.15 Å/s. The total nominal thickness of the film was approximately 11nm (10nmHfO2/1nmDy_2O_3). MIS capacitors were prepared by shadow mask and e-beam evaporation of 30-nm-thick Pt electrodes to define circular dots, 300 μm in diameter. The back ohmic contact was made using eutectic InGa alloy.

The devices have been subjected to electrical stress under CVS conditions with the Keithley 617 meter. We took successive stresses of 1000s at two different fields (3MV/cm, 4MV/cm). After each stress cycle the gate bias was interrupted for a while in order to measure current density-gate voltage (J_g-V_g) and current density-stress time (J_g-t) curves, with the simultaneous acquisition of a high frequency (*hf*) capacitance– voltage (*C-V*) curve for the determination of the flatband voltage shift (ΔV_{FB}) by using a pulsing technique (also known as 'stress and sense'), more details are described elsewhere [30]. The *C-V* measurement was obtained using an Agilent 4284A LCR meter. Fresh devices were used for each stress measurement.

5.4 Results and discussion

The current density (J_g) as function of time (t) is shown in Fig. 1(a) at CVS condition, where constant stress field is 4MV/cm and the solid line is used as a guide line to the eye. The experimental result shows initially the current density (J_g) decrease until to a turn around point, after that it follows an increase of J_g, finally reaches a saturation value of J_g with respect to stress time (t). The possible explanations of Fig.1 are following:

(i): we observed in the first few seconds a decrease of current and then an increase of stress current, the current passes through a minimum, which could seem to indicate the creation of positive charges as well as filling at the pre-existing fixed oxide traps, responsible to the decrease of current. After a few seconds of stress it reaches to a turn-around point, and then the creation of negative charges (bulk/interface) responsible for the J_g increase. Eventually after long time stress it reached to breakdown (BD). To see the BD mechanism quite a long time is needed, the result is not shown here. We conclude that the creation of new defects are gradually increasing and then slows, finally the upward exponential curve reaches saturation.

(ii) This could also be explained with two simultaneous mechanisms together, namely, Maxwell–Wagner instability [29] and relaxation effect of the bilayers [31].

This metal-oxide high-κ behaviour is contributed by dielectric polarization/relaxation and charge trapping/detrapping together. In the experimental data, the J_g noise level could be explained with the above mechanism Maxwell–Wagner instability [29] that we have detailed before. While at low stress field (3MV/cm) we notice the slight decay of current with respect to stress time (Fig.1b). The change of the J_g is almost negligible, could be a random trapping/detrapping mechanism and after 479s we notice a sudden increase of J_g may a soft breakdown (SBD), finally J_g remains the same leakage level.

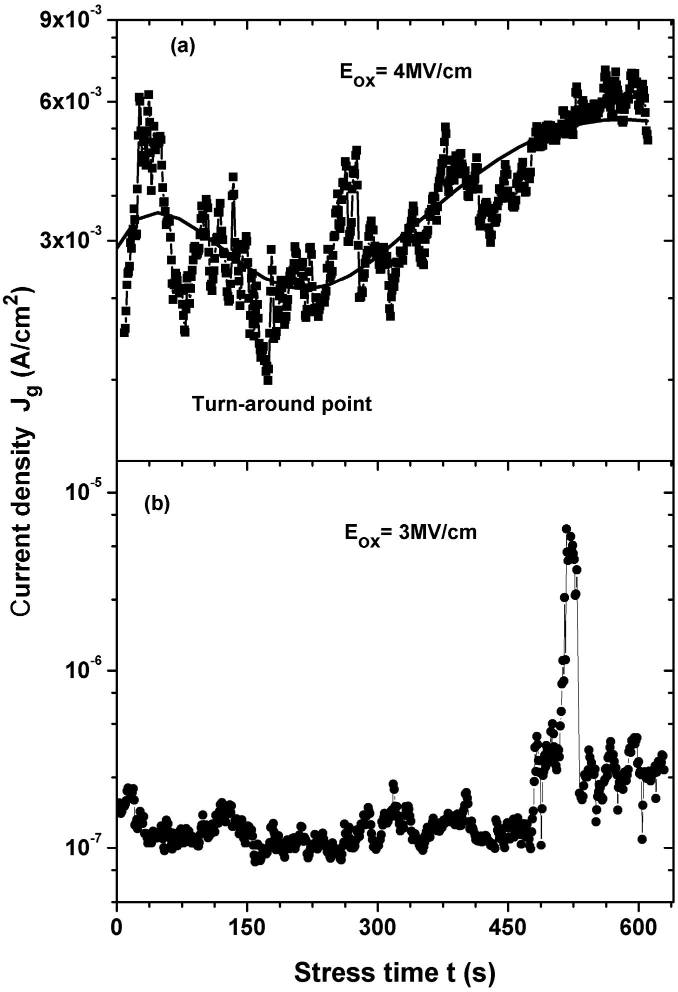

Fig. 1: *The Fig.1 (a) shows current density (J_g) versus stress time (t) graph at high field. Initial current decrease and final transient increase are observed. The solid line is guide line to the eye. While a J_g as a function t at low stress field displays in Fig 1(b).*

After a quite long time J_g starts increasing, the result is not show here. Interesting thing that we have noticed in the measurement is sometime the J_g increases and sometime decreases keeping the current leakage level almost of the same order could be referred as noise; basically the J_g trend is decreasing with respect to stress until a long stress time, which is not fully understood. This could be explained as contributions of both relaxation and Maxwell–Wagner instability together [32]. The charges are accumulated at the interface of the gate stack; suddenly find a percolation path causes increase of J_g and/or detrapping path decreases J_g.

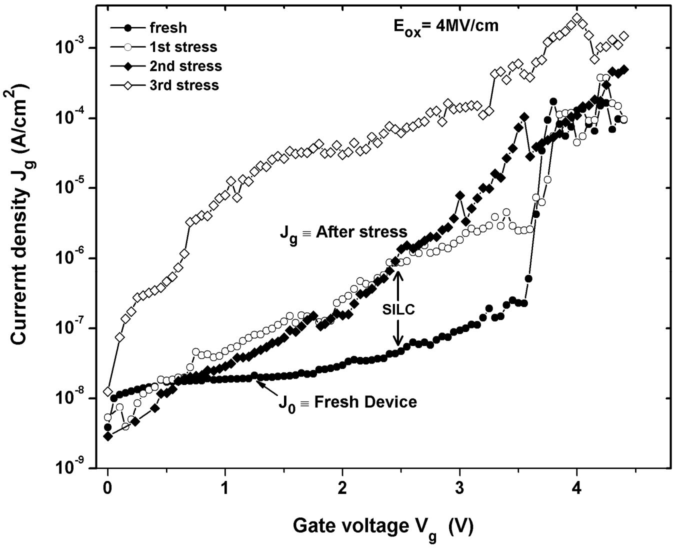

Fig. 2: *The figure shows the gate current density J_g vs bias V_g before and after high uccessive stress.*

Stress induced leakage current (SILC) through the gate dielectric of a MOS capacitor causes an additional power consumption which, although tolerable in currently used technologies, is unwanted especially in low-power applications; there it may become a reliability issue in those deep-submicron technologies where SILC dominates over tunnelling current. We have introduced previously CVS and SILC. The CVS method [1, 5, 15] was used to study the SILC at various stress fields (E_{ox}) with respect to time. Two different stress fields (3MV/cm and 4MV/cm) were applied on the same area of 7x10^{-4} cm^2 of different capacitors successively, immediately after each stress the leakage current density (J_g) as a function of gate voltage (V_g) i.e. J_g-V_g curves were also measured. Fresh capacitors were used for these measurements during each different stress field.

Gate current density (J_g) as function of applied gate voltage (V_g) are shown in Fig.2, where J_g-V_g curves were taken after each stress of 1000s at 4MV/cm. The increase of current density is distinctly exemplified after each stress and from the curves we notice SILC. It is the increase in low-level leakage across a thin gate oxide after the oxide has been subjected to a high electrical-field stress. SILC (J_{increase}) can be given by J_g-J_o, where J_o and J_g are the gate current densities at a given bias before and after stressing the device respectively. However the different behaviour was observed at low stress field (3MV/cm) case which is illustrated in Fig. 3 where shows J_g-V_g curves of fresh and after successive stresses on the device. Here we have observed that the current decreases slightly as function of stress time (i.e. charge injection), resulting in negligible and insignificant SILC. So that infers SILC is field dependent, i.e. at high stress field creation of new defects is evident [9] and on the other hand, at low field it explains anomalously [33]. This means that there is no SILC at low stressing which perhaps is opposite from higher stress; and that SILC contributes mostly in gate leakage current. Also it is worth mentioning that the leakage current density at 1V±V_{FB} is found to be around ~10^{-8}A/cm^2, which is very low level leakage current indicating a good integrity of the gate stack.

When the applied CVS field is low (Fig. 3), we have observed that SILC is slightly decreasing, virtually is negligible. Two mechanisms can be claimed as responsible for SILC decay [29]: *(a)* "clogging" of oxide neutral defects and *(b)* trapping of negative charge in the bilayer interfaces. Based on the first mechanism, electron trapping could likely occur just on the weak spots, which arbitrate SILC. Later, a local relaxation of oxide lattice may lead to the annealing of the defect, resulting in the either weak or strong bond. It is also possible that relaxation could result in such a deep trap, that electrons are no longer available for SILC conduction. Alternatively, electrons could be trapped also by deep defects other than those directly involved in the tunnelling transport.

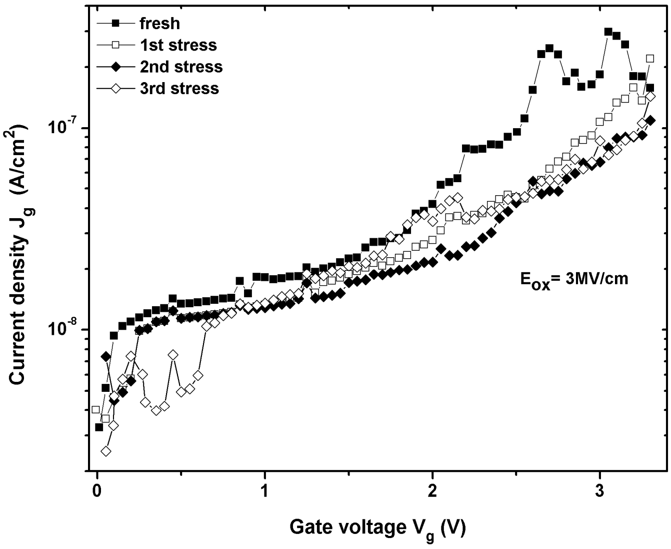

Fig. 3 . *Typical J_g-V_g curves plotted before and after a low stress field and it reveals negligible SILC values.*

The SILC generation kinetics follows a universal power law [34].

$$\delta \ln(J_{SILC}) / \delta Q_{inj} = K_e N_{inj}^{\nu} \quad , \tag{5.1}$$

where, K_e is a parameter that depends on oxide thickness and oxidation technology, $N_{inj}=Q_{inj}/q$; N_{inj} is the number of injected charge, Q_{inj} is the total charge injected, q=1.6x10^{-19}C is the elementary charge, where the injected charge (Q_{inj}) is calculated from the fundamental equation:

$$Q_{inj} = \int_0^t J_g(t)\, dt \quad , \tag{5.2}$$

here, J_g is current density. The kinetics law applies to all constant voltage stressed devices, regardless of their oxide thickness or oxidation process. Integrating Eq. (5.1) we find

$$J_{SILC} = J_{sat} \exp\left(-D / Q_{inj}^{a}\right) \tag{5.3}$$

in which, $\alpha = -(v-1)$, $D = K_e/\alpha$, while J_{sat} is an integration constant. The power law describes well the experimental behavior of SILC, predicting saturation at a value J_{sat}.

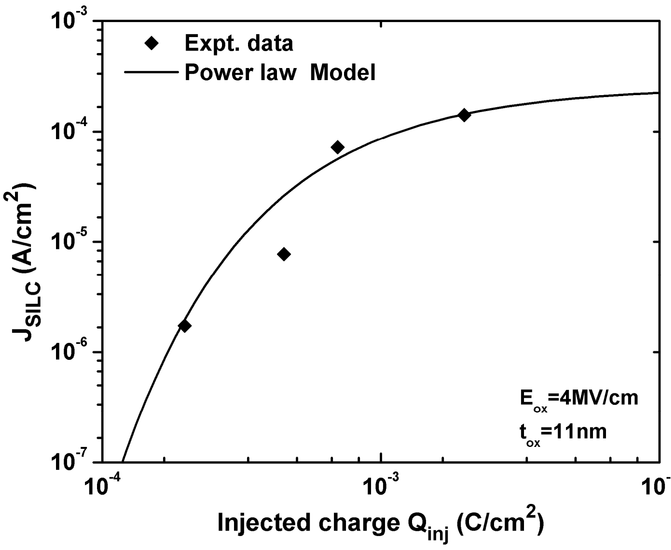

Fig. 4: *Experimental data of SILC (symbol) and corresponding simulation (solid line) obtain from Power Law Model (Eq. 5.3) after CVS at 4MV/cm.*

for high injected charges. The parameter K_e appearing in Eq. (5.1), and also in D in Eq. (5.3), is related to the growth rate of SILC. Fig.4 shows the stress induced leakage current (J_{SILC}) versus injected charge (Q_{inj}) during the stress. We use Eq. (5.3) to fit our experimental data (Fig. 4). The value of v is found to be -1.37 for oxide thickness t_{ox}=11nm while the value of v has been reported from -1.1 to -1.4 [16, 34].

Stress induced leakage current is used to monitor the oxide degradation and to predict the oxide's behaviour under low voltage stress. Oxide degradation is usually quantified by the normalized excess SILC ($\Delta J/J_O$) due to stress; also it is related to the injected charges across the gate dielectrics. The normalized current density increase is defined as $\Delta J/J_o$, where $\Delta J = J_g - J_o$. One observes for different stress voltages that $\Delta J/J_o$ changes (increases or decreases) with respect to the injected charges and follows a power-law [35]

$$\Delta J / J_O = B Q_{inj}^{\gamma} \tag{5.4}$$

where, B and γ are SILC related parameters obtained from our experimental data. B is the leakage current cussed by the traps generated during stress and γ corresponds to the trap generation rate. The normalized excess gate leakage current ($\Delta J/J_o$) is plotted as a function of injected charge (Q_{inj}) at two different gate stress voltages. Each CVS was performed at room temperature. Initially, at high field, in log-log plot, SILC increases linearly. Following a large electrons injection (long stress time), usually SILC reaches to saturation. In the figure, at high field (4MV/cm), SILC doesn't reach perfect saturation; the injected charge is perhaps too low. But, it interesting to note in Fig.5, at low stress field, we do not observe SILC variations, i.e. equal to 0, so we may conclude SILC is almost negligible. Eventually, at low field, DiMaria [14] did not observe saturation of SILC not even a decrease.

It was also reported initially the SILC was increasing linearly with electron fluence; at large fluence the saturation of SILC was observed. In our study, as the positive high gate voltage is applied, a large number of traps (or broken bonds) are generated within the gate dielectric

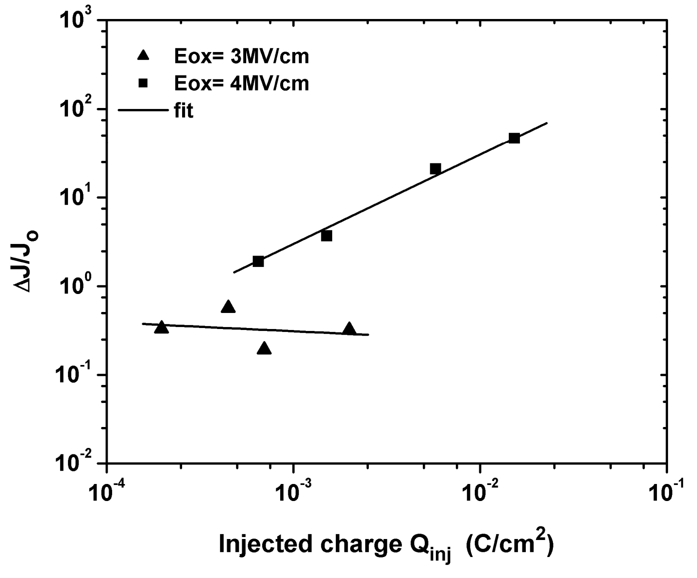

Fig. 5: *Normalized leakage current ($\Delta J/J_O$) versus injected charge Q_{inj}, measured at two different electric fields (4MV/cm & 3MV/cm) after successive stress of 1000s with CVS methods. Symbols indicate the experimental data and solid lines the fit by Eq. (5.4).*

layer and in the interface [36]. We assume that these traps are randomly occupied within the oxide. When a critical number of traps are generated, they will form a percolation path between the gate and the substrate, leading to a sudden increase in gate current which may cause oxide breakdown [37]. In addition, the electrons injected from n-Ge substrate get trapped in the pre-existing traps in the oxides. Under the long stress time, the number of unoccupied trap states available for electron trapping will decrease and the decreased number of available traps will reduce the net trapping rate so that the SILC becomes saturated after the initial stress time [33]. Fitting Eq. (5.4) to the experimental data we have found the value of γ for 3MV/cm and 4MV/cm to be -0.1 and 0.89 respectively. So, at low field the negative value indicates the creation of a few interface traps and the pre-existing traps at the interface of the gate stacks are filling-up; as a result, there are not enough defects/traps available. On the contrary, at high field it indicates a high rate of creation of new traps in the bulk of the oxide.

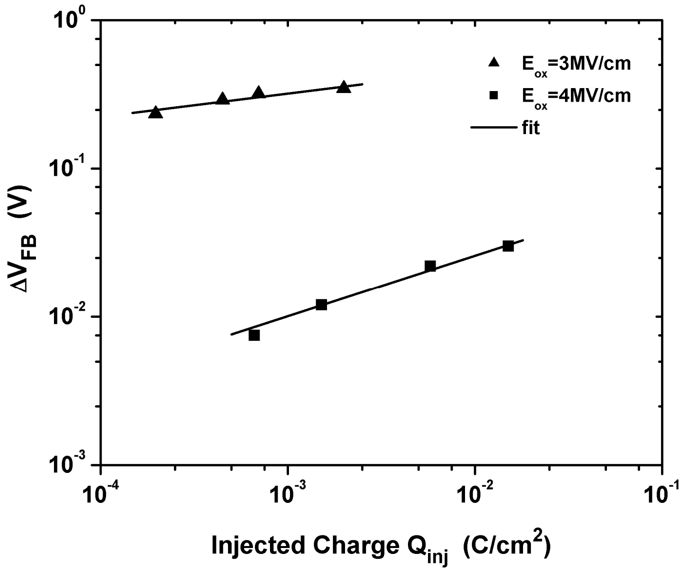

Fig. 6: *Flatband voltage shifts ΔV_{FB} versus injected charge fluence Q_{inj} at two CVS electric fields (3MV/cm & 4MV/cm). Symbols indicate the experimental data and solid lines the fit by Eq. (5.5).*

Maserjian and Zamani reported that charge assisted tunneling by the charge build-up in the oxides resulted in excess current during stressing [8]. The oxide trap charge build-up (Q_{ot}) can be measured from the flatband voltage shift, using hf *C-V* technique. It has also been reported that flatband voltage shift (ΔV_{FB}) is a tool to calculate the trapped charge ($Q_{ot} = \Delta V_{FB} C_{ox}$ [38], where C_{ox} is oxide capacitance) in the bulk of the oxide during CVS [39]. In analogy to Eq. (5.4), the flatband voltage shift and injected electron fluence can be expressed as empirical power-law according to *Kumar* [39] as:

$$\Delta V_{FB} = \Delta V_{\max} Q_{inj}^{\delta}, \tag{6.5}$$

here, ΔV_{max} is a constant, which is defined as the maximum flatband shift during each stress and δ is the exponential power. Fig. 6 displays the flatband voltage shift (ΔV_{FB}) as a function of injected electron fluence (Q_{inj}) at two different fields, which investigates the oxide charge build-up [15]. At low field (3MV/cm) ΔV_{FB} is higher than that of high field (4MV/cm). So at low field more negative charges are trapped although at higher field the charge trapping is less. During low stress field the charge build-up is dominant process to the creation of new traps/defects, while at higher field the charge trapping mechanism is rather faint. Fitting Eq. (5.5) to the experimental data, we found the δ values to be 0.15 and 0.41 for 3MV/cm and 4MV/cm respectively. The compatible results (δ = 0.1 ~ 0.9) have been reported from other researchers [40-42]. In a recent work [30], it was reported that at higher stress field the amount of trapped charge is more than that of at low stress field, which is different from our present work. It is not quite understandable, could be that the present dielectric is gate stack (HfO_2/Dy_2O_3) while other was single layer (CeO_2). It is also noticeable that the amount of trapped charges of the present gate stack is lower than that of CeO_2 single layer. As we mention before, due to different-κ dielectric layers there was present the Maxwell–Wagner instability and in the same time because of the gate stack of high-κ HfO_2 (κ~25) with Dy_2O_3

(κ~12-14) the relaxation effect was present. We have noticed that at low stress field the relaxation is more effective mechanism in this gate stack [32]. However, in this structure of gate dielectrics there were basically three layer e.g. germanate (Dy-Ge-O), Dy_2O_3 and HfO_2 (result is not shown here), so finally there were three interface where the charge trapping was dominant mechanism. Similar relaxation effect was also observed in other gate stacks e.g. HfO_2/SiO_2 [22, 29], $ZrHfO/SiO_2$ [31].

5.5 Conclusions

In the present work we have investigated reliability issues of the gate stack of HfO_2/Dy_2O_3 namely stress induced leakage current, flatband voltage shift and charge trapping in the interface of bilayers. It was the first time, to our knowledge that this gate stack on Ge substrate was studied. The value of leakage current density at $1V \pm V_{FB}$ was extremely low ($\sim 10^{-8}A/cm^2$), which indicates good dielectric property of the gate stack. Studying SILC we found that at high field it increases and obeys a power law; on the contrary, at low field it was not visible. Moreover, at high field, initially (under CVS) there was more charge trapping at the pre-existing traps at the bulk/interface followed by the creation of interface defects and later was the creation of a large number of neutral defects which cause SILC. This elucidates the correlation of charge build-up and SILC. We have found from our study that at low stress charge trapping is a dominant process over SILC, while at high stress field situation reverses i.e. charge trapping is faint but SILC is prevailing. The characteristic SILC phenomenon is observed regardless of substrates (either Si or Ge) and has a similar behaviour. The power law models of SILC proposed for Si-substrate could be used for Ge substrate. From the experimental evidence, low SILC betokens for the future high performance, reliable gate stacks for CMOS Technology.

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Chapter 6

“Investigation of voltage dependent relaxation, charge trapping and stress induced leakage current (SILC) effects in HfO_2/Dy_2O_3 gate stacks grown on Ge (100) substrates”

6.1 Motivation

In this chapter we investigate the voltage dependent relaxation effects and charge trapping characteristics of Pt/ HfO_2/Dy_2O_3 /p-Ge MOS devices. The devices have been subjected to constant voltage stress (CVS) and show relaxation effects in the whole range of applied stress voltages (-1 to -5 V). We observe charge trapping is negligible at low stress field while at higher fields (>4MV/cm) it is significant. Also interesting is the fact that the trapped charge is negative at low stress fields but changes to positive at higher fields.

6.2 Introduction

Although the initial transistors were germanium-based, over the last four decades silicon is the most widely utilized semiconductor for electronics. Pure Ge offers 2χ higher mobility for electrons and 4χ higher mobility for holes with compared to Si. In order to keep up with scaling requirements set by ITRS, gate dielectrics with higher (~25) permittivity, like HfO_2, are used as a replacement of SiO_2 [1]. Germanium is highly reactive with HfO_2, which may lead to Ge diffusion into the HfO_2 dielectric [1]. One possible solution is the use of rare earth oxide dielectrics as passivation layers, which are "friendly" with Ge and can be directly deposited on it [2], capped with a higher-k dielectric to improve scalability. It has been shown that Dy_2O_3 can efficiently eliminate Ge diffusion originating either from the substrate or interfacial layer. It also reduces the charge trapping effects while improving the Equivalent Oxide Thickness (EOT) [3].

Another serious problem that arises when gate stacks of high-k dielectrics are used in MOS devices is that they all produce electrical instabilities in MOS devices [4]. This is a major device reliability issue since it causes threshold voltage (V_{TH}) shifts and drive current degradation over device operation time. Many of these instabilities could be interpreted as arising from the trapping of charge somewhere within the gate stack. In particular, the high-speed experiments of *Kerber et al.*[5-6] seem to paint a vivid picture of electrons filling up a gate stack when a gate bias is applied, then rushing out after the bias is removed, producing dramatic instabilities in the drain current of transistors at short timescales. By cycling the gate voltage on and off [4-6], one also observes gradual shifts in the properties of devices, implying that the electrons that flow into the gate stack while the bias is on do not have time to flow out completely when the bias is off. For high-κ gate stacks to be suitable for commercial devices, these electrical instabilities must be eliminated, so it is imperative to understand why charge trapping takes place.

Two effects are known to produce such instabilities in MOS devices, namely the Maxwell-Wagner instability and the relaxation effects of the various gate dielectrics. They both give a $J \sim t^{-n}$ behavior which is strongly voltage dependent [4-7]. Moreover; they are usually both present at the same time making the corresponding analysis a very complex task. This is also the main subject of the present work. The studied Pt/ HfO_2/Dy_2O_3 /p-Ge MOS devices have been subjected to constant voltage stress (CVS) conditions at accumulation and they show Maxwell-Wagner instabilities and relaxation effects as well as charge trapping at pre-existing bulk oxide defects.

6.3 Experimental

Dy_2O_3/HfO_2 oxide stacks were prepared by atomic oxygen beam deposition on p-type Ge (100) substrates. Native oxide was desorbed *in-situ* under UHV conditions by heating the substrate to 360°C for 15 minutes, until a (2x1) reconstruction appeared in the (RHEED) pattern, indicating a clean (100) surface. Subsequently, the substrate was cooled down to 225°C where the oxide stacks were deposited. The surface was exposed to atomic O beams generated by an RF plasma source with the simultaneous e-beam evaporation of Dy/Hf at a rate of about ~0.15 Å/s. Two different samples were prepared for the present study. Sample A had a single (~10nm thick) Dy_2O_3 layer while the total thickness of the dielectrics of sample B was approximately 7nm (5nm HfO_2 / 2nm Dy_2O_3). MIS capacitors were prepared by shadow mask and e-beam evaporation of 30-nm-thick Pt electrodes to define circular dots, 200 μm in diameter. The back ohmic contact was made using a eutectic InGa alloy.

The devices have been subjected to electrical stress under CVS conditions at accumulation. Successive stress cycles of 500s at different gate voltages were applied with the Keithley 617 meter which was also measuring the corresponding current with time. After each stress cycle the gate bias was stopped in order to measure either the current-voltage (I_g-V_g) curves or the high frequency (f=100 kHz) capacitance-voltage (*C-V*) curve for the determination of the flatband voltage shift (ΔV_{FB}). The latter measurement was obtained with the Agilent 4284A *LCR* meter.

6.4 Results and Discussion

Typical *C-V* curves of the MOS capacitor with the gate stack dielectric are illustrated in Fig.1 (a, b). In order to measure the trapped oxide charges immediately after stopping the stress pulse, the curves were obtained from accumulation to inversion and backwards. Nevertheless, the important electrical properties of the capacitors do not show substantial differences from the C-Vs acquired in the opposite way (i.e. from inversion to accumulation and backwards). Taking into account quantum mechanical corrections, the calculated *EOT* values were 2.68nm and 1.93nm for sample A and B respectively. The hysteresis of *C-V* curve was rather large (around 400mV at midgap) and a large density of slow interface traps is evident even at ac signal frequencies as high as 100 kHz. The corresponding current-voltage (*I-V*) curves show very small leakage currents (around 10nA/cm^2 @ V_{FB}-1V). Important information comes from the structural analysis of the films which evidences the presence of a thin amorphous interfacial layer consisting mainly of Ge-O-Dy phases. Hence both samples must be considered as gate stacks.

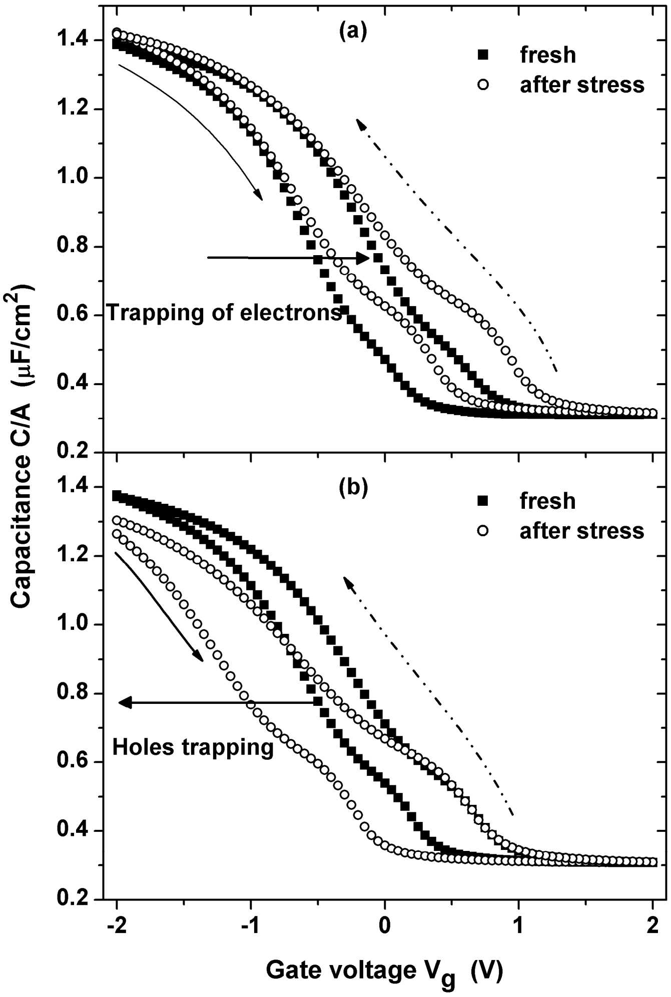

Fig. 1: *High frequency C-V (f=100 kHz) before and after the application of ten consecutive CVS cycles of 500s each on sample B (Pt-5nm HfO_2 / 2nm Dy_2O_3/p-Ge). Stress voltage is low in (a) a moderate in (b). Positive V_{FB} shifts in (a) indicate trapping of electrons in the bulk of the oxides while negative shifts in (b) indicate the oppositely.*

The interesting result from the analysis of the high frequency *C-V* curves (Fig. 1(a, b)) is that when the applied stress voltage is rather low, the trapped charge in the oxide is negative (i.e. ΔV_{FB} shift is positive) while at moderate stress voltages the relevant negative shift of the *C-V* curves indicates positive charge trapping. The same results have also been obtained for the single Dy_2O_3 layer. There are two possible explanations of the observed phenomenon:

a) As the gate voltage during the stress pulse is always negative, electrons are injected into the dielectrics from the metal. At low voltages these electrons are trapped in pre-existing defects and the fields across each dielectric are not high enough for these electrons to escape towards the *p*-Ge substrate (assuming the usual Poole-Frenkel or Trap Assisted Tunneling transport). At higher stress voltages the situation is different in the sense that even the electrons already trapped in the oxides are able to escape towards the substrate, thus leaving a net positively charged dielectric.

b) The fact that the two layers of a high-*k* gate stack are different materials means that they also have different conductivities. Then, the application of a gate bias will immediately produce a discontinuity in current density at the interface between the two layers, causing charge to accumulate there until, in steady state, the same current density (J_e) flows through both layers. If the gate bias is removed, a discontinuity in current density will again be produced, this time causing the charge to rush out of the gate stack [4]. Another aspect worth noting is that, because the conductivities of HfO_2 and Dy_2O_3 thin films depend differently on field, either layer can have the higher conductivity, depending on the choice of gate voltage. Frohman-Bentchkowsky and Lenzlinger [8] caused the sign of the trapped charge to switch by varying the gate voltage of similar (gate stack) structures. This effect was predicted from the independent measurements of the conductivities of the two layers [4, 8]. A similar change of sign might have already been observed in HfO_2/SiO_2 gate stacks.[8] Furthermore, in a previous work [9], we observed the same effect on MOS devices with CeO_2 as the gate dielectric.

In order to understand better which mechanism is responsible for the voltage dependence of ΔV_{FB}, the transient response of the current during the application of the stress pulse was measured. Figure 2(a, b) illustrates the current density J_e versus stress time t curves after the application of low gate voltage pulses on both samples. It is evident that in all cases the decay of current follows a t^{-n} law with n values ranging from 0.5 to 1. Additionally, the n values increase after each new stress cycle reaching a value of 0.9 after 10 cycles. The fact that the

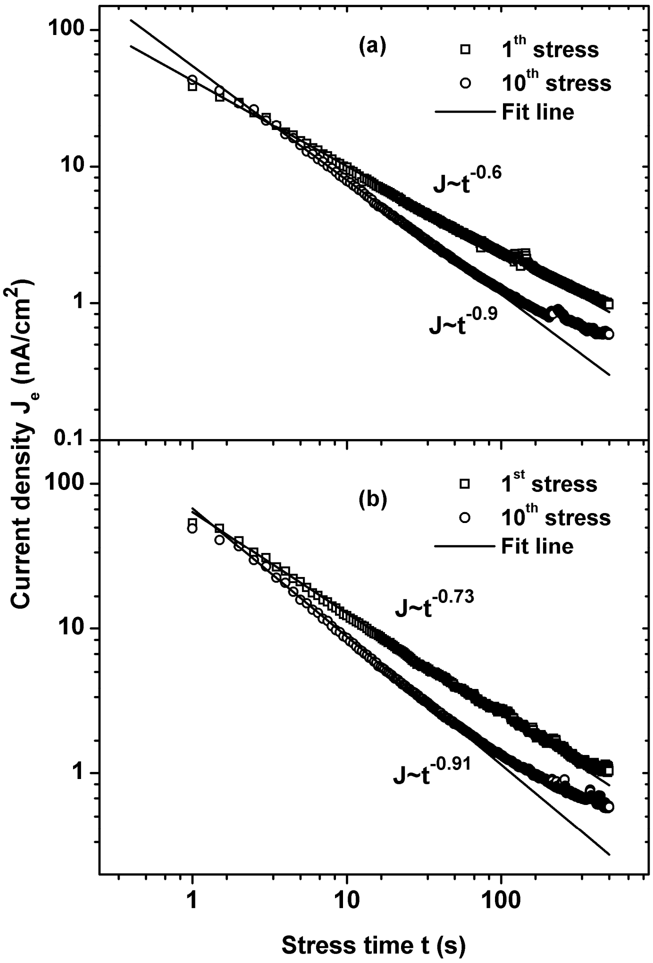

Fig. 2: *The figures illustrate absolute current density J_e as a function of stress time t. Comparison of transient current behavior during the application of the first and the 10^{th} stress pulse. The applied gate voltage bias and the corresponding fields are low for both samples (A & B). The solid lines show the corresponding t^{-n} behavior.*

initial value is far from unity indicates that a Maxwell–Wagner instability (following the terminology used in [4]) is present along with the usual dielectric relaxation of the high-κ dielectrics. In the latter case the relaxation current decays with time following the Curie-von

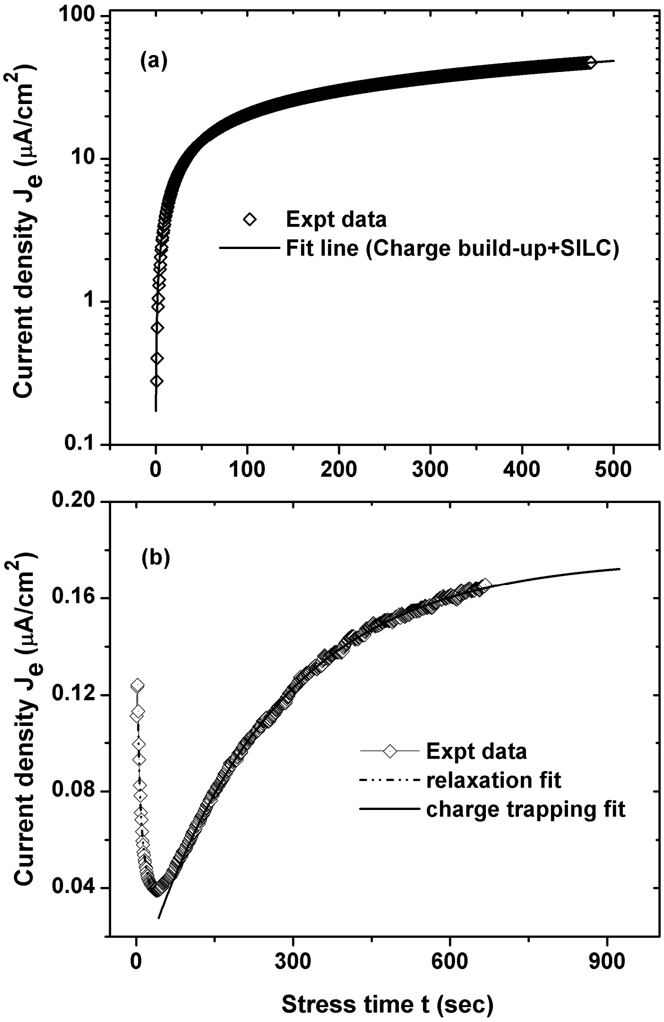

Fig. 3: *Figures show the absolute J_e vs t, the comparison of the transient current behavior during the application of a stress pulse at a higher gate voltage bias so that the corresponding fields are moderate for both the samples A & B (figures a & b respectively). The solid lines are best fit to the experimental data according to a model described in the text.*

Schweidler law[10]: $J_e/P=\alpha t^{-n}$, where J_e is the relaxation current density (A/cm^2), P is the total polarization or surface charge density (V nF/cm^2), α is a constant in seconds and n is a real number close to 1. The gradual increase of n could be attributed to the fact that the Maxwell–Wagner instability becomes less important after each stress cycle and the relevant J_e values decrease so that, after 10 consecutive cycles, it is the dielectric relaxation current that dominates. One reason for that is the gradual change of the conductivities of the various dielectric layers due to charge trapping in preexisting bulk oxide defects. Another observation supporting the above analysis is the fact that the initial n value of sample B is considerably higher than that of sample A. The former structure contains a HfO_2 layer with a higher dielectric constant (κ~25) than that of Dy_2O_3. Therefore the dielectric relaxation effects are expected to be stronger in the case of sample B.

The situation is different at higher applied voltages. As illustrated in Fig.3, the application of moderate to high stress voltages does not result in relaxation effects for the MOS device with the single Dy_2O_3 film (sample A). The transient current behavior is now governed by charge trapping at preexisting bulk oxide defects. On the contrary, application of similar stress voltages on the capacitor with the HfO_2/Dy_2O_3 stack show the coexistence of all different mechanisms separated only by the different time scales of each one. Therefore, during the first 32 seconds after the application of the pulse the current density J_e decreases with time due to the relaxation mechanisms, following a t^{-n} law with n values as low as 0.5. At the same time the magnitude of the leakage current that flows through the dielectrics is 2-3 orders of magnitude higher than in the case of low stress voltages. Therefore the charge trapping effects become more significant and the J_e values start to increase following a model originally proposed by *Nigam et al.*[11] to explain charge trapping in MOS devices with thin gate stack dielectrics. According to this model, the transient behavior of J_e with time of sample A (Fig.3a), can be explained by taking into consideration both trapping on preexisting bulk oxide defects (with a characteristic time constant τ) as well as creation of new defects due to electrical stressing (which follow a power law $J_e \sim t^{\delta}$). However for sample B, only charge trapping must be considered for best fitting of the experimental data (Fig. 3b). In addition, the time constant τ is one order of magnitude greater ($\tau \sim 260$s) for sample B than for the structure containing only Dy_2O_3. This is an interesting result as it shows that there are different types of defects in the two oxides. Furthermore, the overall better insulating properties of HfO_2 are confirmed as

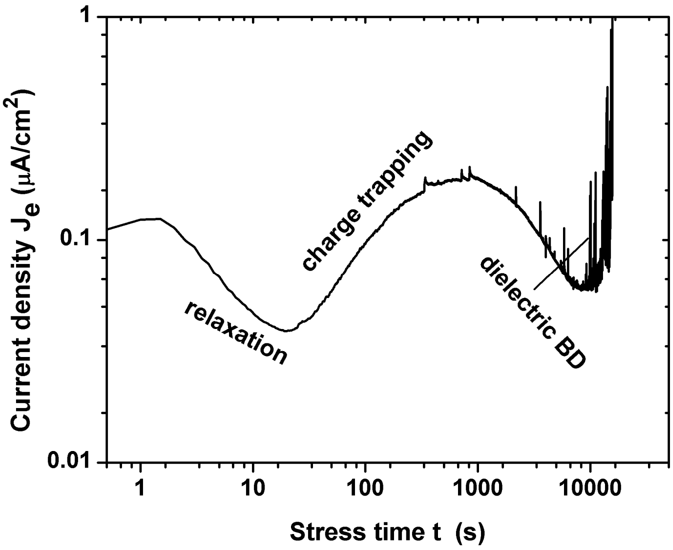

Fig. 4: *Current density J_e as a function of stress time t for sample B at moderate/high CVS conditions applied for very long times. The device shows initially relaxation behavior, then (for t>90s) charge trapping to the preexisting traps in the oxide takes place which eventually leads to breakdown.*

sample B, although stressed at slightly higher electric fields, shows negligible rate of creation of new defects. Finally both devices have been subjected to very long CVS conditions at moderate gate voltages. Figure 4 shows that sample B reaches hard breakdown after a number of soft breakdown events and a total stress time of 18000s. On the contrary the single Dy_2O_3 layer (not shown here) required substantially longer periods of time in order to collapse which is probably attributed to the different breakdown mechanisms occurring in the two oxides. One possible explanation is that in the case of the gate stack dielectric one of the oxides (most probably the thinner Dy_2O_3) goes to breakdown first, leading to a major redistribution of the corresponding fields. Thus the field across the other dielectric (HfO_2) increases abruptly leading to a second relaxation effect. This time soft breakdown (SBD) effects appear which eventually lead to a hard breakdown of the second layer and the MOS capacitor itself. Nevertheless this effect needs to be studied in more detail.

6.5 Conclusions

Charge trapping and relaxation characteristics of Pt/ HfO_2/Dy_2O_3 /p-Ge gate stacks were studied by means of CVS measurements. At low applied stress voltages two independent electrical instabilities were observed, namely the Maxwell–Wagner instability and dielectric relaxation. While both effects were present simultaneously, the increase of the applied voltage and/or the repetition of the stress cycles lead to a change of the relative magnitude of each one separately.

Another aspect of the studied structures worth noting is that because the conductivities of HfO_2 and Dy_2O_3 thin films depend differently on field, either layer can have the higher conductivity, depending on the choice of gate voltage. Then, by varying the gate voltage, the sign of the trapped charge switched from positive to negative, an effect that was predicted but rarely reported for high-k gate stacks.

Finally, at moderate to high stress fields the dominant process is charge trapping and creation of new defects (SILC). The analysis of the transient behavior of the current density in this case revealed the existence of two different trapping centers in the two dielectrics at least in terms of the relevant capture cross sections.

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Chapter 7

Conclusions

In the present thesis reliability issues as well as electrical characteristics of rare-earth oxides (REOs) and their gate stacks grown on Germanium substrates have been investigated.

Reliability issues such as charge trapping characteristics, stress-induced leakage current (SILC), dielectric degradation, dielectric relaxation, Maxwell-Wagner instabilities are studied applying a 'stress and sense' technique. It very important to note that the charge trapping is dominant mechanism at low stress field in CeO_2 while at higher filed SILC was important. The capture cross section of the traps to be around -10^{-18}~10^{-19} cm^2 signifies the traps are neutral and deep traps. The charge trapping and SILC are simultaneous effects when the device is under bias, while the device under bias, yet they are quite different from those observed on Si/SiO_2 structures. The important findings are the charge trapping effect in CeO_2/Ge device is on the order of six times more that observed in Si/SiO_2. It is found that at higher field the SILC is significant while at low field it is negligible. Also it is reported that charge trapping and SILC effects can be well described by the Nigam model. Also current conduction mechanisms in CeO_2 have been reported and Schottky emission describes at low stress field as the band gap of CeO_2 is low (3.3eV), on the other hand the conduction mechanism at higher field is Poole-Frenkel mechanism. The Schottky emission barrier height for CeO_2 is found to be 0.91±0.02eV while trap depth is around 0.6±0.03eV.

The stress-induced leakage current (SILC) is also studied for $Pt/HfO_2/Dy_2O_3/Ge$ devices. The similar result like CeO_2/Ge device is observed, while the SILC follows a power law at higher field. The dielectric relaxation (DR) is investigated in $Pt/HfO_2/Dy_2O_3/Ge$ devices. Usually, DR follows a $\sim t^{-n}$ behaviour when MOS device shows only DR, and the value of *n* is unity. The *n* value found for gate stack (HfO_2/Dy_2O_3) is less than unity (0.7-0.9) during the device under constant voltage stress. One important finding is that DR is not only one single event, and is combined effect together with charge trapping. With the stress time in progress on the devices the charge trapping become important. High-*κ* bilayer gate stack itself is the cause of charge trapping at the interface of the two dielectrics. As gate stacks compose of two different layers, which means that they will also have different conductivities, so charge will accumulate there at the interface between two different dielectrics until, in steady state, the same current density flows through both layers, and this so called Maxwell-Wagner instabilities. It has also been reported that at low stress field the $Pt/HfO_2/Dy_2O_3/Ge$ devices shows DR behaviour while at higher stress fields this is absent; neverthless, at the higher field the charge trapping is prevailing over other mechanisms.

Chapter 8

Future Works

We have indeed proved the simultaneous effects of dielectric relaxation and Maxwell-Wagner polarization are present in Pt/HfO_2/Dy_2O_3/Ge (for both *n* and *p* type) gate stacks. It is very important to study the other gate stacks such as Pt/HfO_2/CeO_2/Ge, Pt/HfO_2/Lay_2O_3/Ge and make a compression among all gate stacks for the same effects. As we observe that the bilayer gate stacks itself is the cause of charge trapping which also causes dielectric relaxation, if these similar effects are also present in other devices, for example, Pt/HfO_2/CeO_2/Ge, Pt/HfO_2/Lay_2O_3/Ge, and then the engineering of gate stacks need to go for further extensive investigation.

A comparative study of charge trapping-detrapping characteristics of rare-earth oxides (e.g. Pt/CeO_2/n-Ge, Pt/Dy_2O_3/p-Ge, Pt/La_2O_3/Ge) is very important as rare-earth oxides are using as interfacial buffer layer in a gate stack grown on germanium substrates (as an alternative new approach) .

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